GaN Reliability and Lifetime Projections: Phase 16

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The rapid adoption of Gallium Nitride (GaN) devices in many diverse applications calls for continued accumulation of reliability statistics and research into the fundamental physics of failure in GaN devices, including integrated circuits (ICs). It is also necessary to look for information from real-world experience that either confirms the laboratory-derived data or opens new questions about mission robustness. This Phase 16 Reliability Report documents continued work using test-to-fail methodology and adds guidelines for improving thermo-mechanical reliability.

FOCUS AND STRUCTURE OF THIS REPORT

Compared to the Phase 15 Reliability Report [1], this version presents expanded data and analysis. It now includes a general overview of the wear-out mechanisms of primary concern for a given application, which is intended as an introduction to readers new to GaN reliability. Section 1 describes the benefits of testing to failure and how this methodology leads to progress in GaN reliability by revealing a device's intrinsic failure mechanisms. Section 2, which is new to this version of the report, describes how to forecast the reliability of a system in a realistic mission profile that combines periods of substantial and minor stress. The fundamental wear-out mechanisms are discussed individually in Section 3. Compared to previous versions of this report, the thermo-mechanical wear-out mechanisms and overvoltage guidelines include significant new material. Finally, Section 4 reports on the reliability of GaN in specific solar, DC-DC conversion, and light detection and ranging (lidar) applications. A method for optimizing solder stencils for reliable assembly is provided in the Appendix (Section 6), which shows how to determine the solder stand-off height of Power Quad Flat No-Lead (PQFN) packaged GaN FETs.

GETTING STARTED WITH GAN RELIABILITY

Gallium nitride (GaN) high-electron mobility transistors (HEMTs) have revolutionized power conversion technology due to GaN's superior material properties, which lead to smaller die size, lower on-resistance, and lower parasitic capacitance than their Si-based counterparts. In recent decades, GaN has been increasingly deployed in advanced applications such as light detection and ranging (lidar) for autonomous and commercial vehicles, rooftop solar panels, DC-DC converters for servers, data centers, satellites, motor drives for drones, robots, and power tools. As an emerging technology, the stability, reliability, and robustness of GaN HEMTs attracts significant attention.

The primary wear-out mechanisms in GaN include voltage related wear-out, current density driven wear-out, thermo-mechanical wear-out predominantly caused by thermal expansion (CTE) mismatch, and mechanical stress wear-out that is more assembly and application related. To understand which wear-out mechanisms are of primary concern for a given application, designers who are new to GaN are directed to Tables 1 and 2. As listed in the "for details" column of Table 2, this report provides experimental studies and theoretical analysis of all major GaN reliability stressors, with results that can differ from traditional Si-based devices.

Application	Package	Gate-related	Drain-related	Current Density-related	Thermo-Mechanical-related	Mechanical Stress-related
DC-DC	CSP		C		A	E
	PQFN		C		B	
Lidar	CSP	D		F		E
	PQFN	D		F		
Solar	CSP				A	E
	PQFN				B	
Motor Drives	CSP	D	C	F	A	E
	PQFN	D	C	F	B	E

Table 1: GaN primary wear-out mechanism and means of avoidance by application and device type. For the meaning of notes A through F, see Table 2.

CSP = chip scale packaged devices PQFN = power quad flat no-lead devices

Note	General Mitigation Strategy	For details, see section
A	Choose suitable underfill	3.4
B	Design an assembly process that leads to a part which lays flat and adheres well to the PCB	Appendix
C	Remain within datasheet V_{DS} limits, with excursions that remain within drain overvoltage specification	3.2
D	Remain within datasheet V_{GS} limits, with excursions that remain within gate overvoltage specification	3.1
E	Adhere to recommended mechanical specifications during assembly and handling	3.5
F	Adhere to Safe Operating Area specifications	3.3

Table 2: GaN Reliability Concerns - Section References

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SECTION 1: DETERMINING WEAR-OUT MECHANISMS USING TEST-TO-FAIL METHODOLOGY

Standard qualification testing for semiconductors typically involves stressing devices at or near the limits specified in their datasheets for a prolonged period, or for a certain number of cycles. The goal of standard qualification testing is to have zero failures out of a relatively large group of parts tested.

This type of qualification testing is inadequate since it only reports parts that passed a very specific test condition. By testing parts to the point of failure, an understanding of the amount of margin between the datasheet limits can be developed, and more importantly, an understanding of the intrinsic failure mechanisms can be found. By knowing the intrinsic failure mechanisms, the root cause of failure, and the behavior of this mechanism over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions (For an excellent description of test-to-fail methodology for testing semiconductor devices, see reference [2]).

As with all power transistors, the key stress conditions involve voltage, current, temperature, and humidity, as well as various mechanical stresses. There are, however, many ways of applying these stress conditions. For example, voltage stress on a GaN transistor can be applied from the gate terminal to the source terminal (V_{GS}), as well as from the drain terminal to the source terminal (V_{DS}). For example, these stresses can be applied continuously as a DC bias, they can be cycled on-and-off, or they can be applied as high-speed pulses. Current stress can be applied as a continuous DC current, or as a pulsed current. Thermal stresses can be applied continuously by operating devices at a predetermined temperature extreme for a period of time, or temperature can be cycled in a variety of ways.

By stressing devices with each of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test can be determined. To generate failures in a reasonable amount of time, the stress conditions typically need to significantly exceed the datasheet limits of the product. Care needs to be taken to make certain the excess stress condition does not induce a failure mechanism that would never be encountered during normal operation. To make certain that excess stress conditions did not cause the failure, the failed parts need to be carefully analyzed to determine the root cause of their failure. Only by verifying the root cause can a complete understanding of the behavior of a device under a wide range of stress conditions be developed. As the intrinsic failure modes in eGaN® devices are better understood, two facts have become clear; (1) eGaN devices are more robust than Si-based MOSFETs, and (2) silicon MOSFET intrinsic wear-out models do not generally apply when predicting eGaN device lifetime under extreme or long-term electrical stress conditions.

Table 1-1 lists in the left-hand column all the various stressors to which a transistor can be subjected during assembly or operation. Using the various test methods listed in the third column from the left, and taking devices to the point of failure, the intrinsic wear-out mechanisms can be discovered. The wear-out mechanisms confirmed as of this writing are shown in the column on the right.

Stressor	Device/ Package	Test Method	Intrinsic Wear-out Mechanism
Voltage	Device	HTGB	Dielectric failure (TDDB)
			Threshold shift
		HTRB	Threshold shift
			$R_{DS(on)}$ shift
		ESD	Dielectric rupture
Current	Device	DC Current (EM)	Electromigration
			Thermomigration
Current + Voltage (Power)	Device	SOA	Thermal Runaway
		Short Circuit	Thermal Runaway
Voltage Rising/ Falling	Device	Hard-switching Reliability	$R_{DS(on)}$ shift
Current Rising/ Falling	Device	Pulsed Current (Lidar reliability)	None found
Temperature	Package	HTS	None found
Humidity	Package	MSL1	None found
		H3TRB	None found
		AC	None found
		Solderability	Solder corrosion
		uHAST	Denrite Formation/ Corrosion
Mechanical / Thermo-mechanical	Package	TC	Solder Fatigue
		IOL	Solder Fatigue
		Bending Force Test	Delamination
		Bending Force Test	Solder Strength
		Bending Force Test	Piezoelectric Effects
		Die Shear	Solder Strength
		Package Force	Film Cracking
Radiation	Device	Gamma Radiation	None found
		Neutron Radiation	None found
		Heavy Ion Bombardment (SEE)	Crystal displacement damage and ionization damage

Table 1-1: Stress conditions and intrinsic wear-out mechanisms for GaN transistors

SECTION 2: USING TEST-TO-FAIL RESULTS TO PREDICT DEVICE LIFETIME IN A SYSTEM

When multiple failure mechanisms or stressors are involved, the total failure rate of a system, commonly known as Failure in Time (FIT), is the sum of the failure rates per failure mechanism [3,4] as shown below,

$$FIT_{Total} = FIT_1 + FIT_2 + \cdots + FIT_i \qquad \text{Eq. 2-1}$$

where FIT is failure in time, which typically represents the number of failures in 10^9 (1 billion) device hours, and the subscript indicates the different failure mechanisms identified.

FIT is inversely proportional to mean time to failure (MTTF) as described by

$$FIT = \frac{10^9}{MTTF} \quad \text{Eq. 2-2}$$

Therefore, by plugging Equation 2-2 into Equation 2-1, the total MTTF can be described by Equation 2-3,

$$\frac{1}{MTTF_{Total}} = \frac{1}{MTTF_1} + \frac{1}{MTTF_2} + \cdots + \frac{1}{MTTF_i} \quad \text{Eq. 2-3}$$

The subscripts are assigned to the reliability stressors that are relevant to the application of interest. Based on Equation 2-3, it is noted that the smallest denominator yields the smallest MTTF and therefore dominates the overall lifetime. It is critical to understand which stressor is the limiting factor in reliability because the weakest link warrants the most consideration during design and operations.

In most applications, devices experience various stress conditions over the course of the entire mission lifespan, including a combination of different bias conditions and different temperature profiles. Each stress condition corresponds to a specific failure rate (failures per unit time), specified as FRa, FRb, …, FRn. The respective duration of each stress condition is denoted as ta, tb, …, tn. Assuming t_total=t_a+t_b+... +t_n is 10^9 hours, the FIT calculation of total number of failures is then generalized for specific reliability stress conditions as

$$FIT = FR_a \cdot t_a + FR_b \cdot t_b + \cdots + FR_n \cdot t_n \quad \text{Eq. 2-4}$$

The time-averaged failure rate FR can be calculated as

$$FR = FR_a \ \frac{t_a}{t_{total}} + FR_b \ \frac{t_b}{t_{total}} + \cdots + FR_n \ \frac{t_n}{t_{total}} \quad \text{Eq. 2-5}$$

which can be simplified by introducing fractional operation time,

$$i = \frac{t_i}{t_{total}} \quad \text{Eq. 2-6}$$

noted as a, b, …, n. The sum of a, b, …, n is 100% which is given in Equation 2-7.

$$a + b + \cdots + n = 100\% \quad \text{Eq. 2-7}$$

Now Equation 2-5 can be simplified to

$$FR = FR_a \cdot a + FR_b \cdot b + \cdots + FR_n \cdot n \quad \text{Eq. 2-8}$$

It is known that the failure rate under each sub-stress condition is inversely proportional to the device lifetime LT [4] when the same number of failures is generated. The relation is shown in Equation 2-9.

$$FR \propto \frac{1}{LT} \quad \text{Eq. 2-9}$$

Plugging Equation 2-9 into Equation 2-8 yields Equation 2-10.

$$\frac{1}{LT_{Total}} = \frac{a}{LT_a} + \frac{b}{LT_b} + \cdots + \frac{n}{LT_n} \quad \text{Eq. 2-10}$$

where LT_{Total} is the total projected lifetime andLT_i is the projected lifetime for each stress condition.

Equation 2-10 captures how a mission profile consisting of more than one stress condition results in a system lifetime. The fractional operation time (a, b, …, n) in the numerators account for the times spent in harsh, moderate, and mild stress conditions.

SECTION 3: WEAR-OUT MECHANISMS

3.1. Gate Wear-Out

3.1.1. Introduction to Gate Wear-Out Mechanisms

GaN transistors devices require a 5 V_{GS} to properly drive the devices, which leaves a small margin from the nominal bus voltage (~5 V) to the datasheet maximum specification ($V_{GS,Max}$ =6 V). Virtually zero (less than one part per million) failure rate is expected if the gate bias is kept less than 6 $V_{GS,Max}$ during the entire mission lifespan of 10–25 years. If the transient overvoltage rings beyond 6 V_{GS}, a 1% duty cycle-based overvoltage specification is supported by data and a method to project the lifetime due to gate overvoltage is developed.

3.1.2. Gate Reliability Model

To understand gate wear-out mechanisms, four groups of representative GaN HEMTs (EPC2212) and 32 devices per group were tested under four different accelerated stress conditions, where the bias voltages of 8 V, 8.5 V, 9 V, and 9.5 V well exceeded the max rated gate voltage ($V_{GS(max)}$) of 6 V. At 9 V and 9.5 V, failures occurred very quickly, but it took significantly longer at 8 V and 8.5 V. After the failures were identified, failure analyses were conducted on a large number of failures at all test voltages, and a consistent failure mode was found. Fig. 3-1 shows the failure mode observed in all failures analyzed. The location of the gate failures is where the silicon nitride dielectric is sandwiched between gate metal and field plate metal.

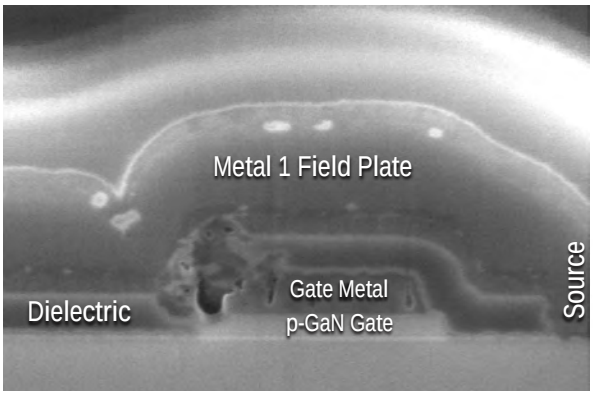


Fig. 3-1. Scanning electron microscopy (SEM) image of a gate failure. Dielectric breakdown is observed between the gate metal and the field plate metal.

To explain all the observations found via failure analysis, an impact ionization model was introduced and developed in a two-step process [1, 5]. Having identified impact ionization as the mechanism responsible for gate wearout led to the development of the following lifetime model applicable to p-GaN gates [5].

$$MTTF = \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \frac{A}{(1-c\Delta T)} exp\left[\left(\frac{B}{V+V_0}\right)^m\right] \quad \text{Eq. 3-1}$$

with parameters listed below:

$m = 1.9$
$V_0 = 1.0\ V$
$B = 57.0\ V$
$A = 1.7 \times 10^{-6}\ s$
$c = 6.5 \times 10^{-3}\ K^{-1}$

The lifetime equation (Equation 3-1) is plotted against measured acceleration data for EPC2212 in Figure 3-2. To produce this fit, all parameters in Equation 3-1 were fixed except A and B. The resulting best fit for B, (when converted into a field by dividing by the gate thickness), resulted in a value of 7.6 x 10^6 V/cm, in very close agreement with Ooi's value of 7.2 x 10^6 V/cm [6].

Figure 3-3 shows the temperature dependence of the lifetime equation at –75°C, 25°C, and 125°C. The temperature dependence (contained in the parameter c) is taken directly from Ozbek [7] without fitting to data. Note that at higher temperature, the MTTF is slightly higher than at lower temperatures, which, although counter-intuitive, is consistent with the measured data reported in the Phase 14 report [5].

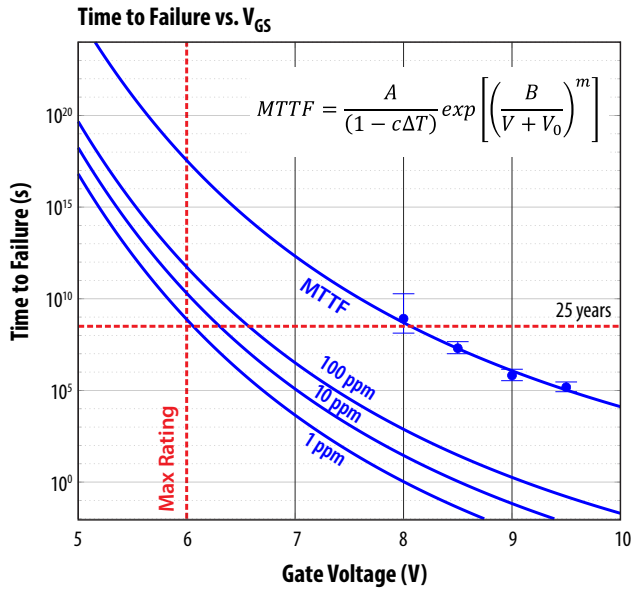


Figure 3-2: EPC2212 MTTF vs. V_{GS} at 25°C (and error bars) are shown for four different voltage legs. The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

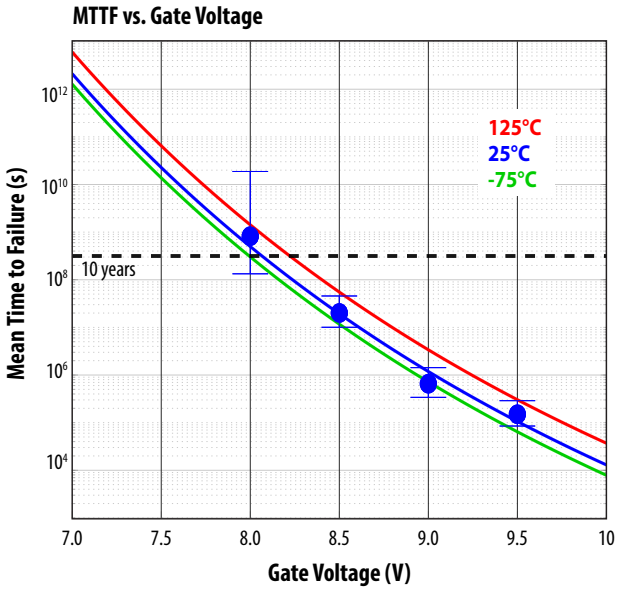


Figure 3-3: MTTF for EPC2212 (25°C) measured at four different gate biases. Blue line is the lifetime model. Red and green lines are predictions of the lifetime model at 125°C and –75°C, respectively.

3.1.3. Summary of Physics-Based Gate Lifetime Model

The impact ionization model of gate lifetime in GaN transistors (Equation 3-1) successfully accounts for a host of observed factors:

- Positive temperature coefficient of MTTF (which is unusual in semiconductor physics of failure).
- Very high acceleration with gate bias, and acceleration that is steeper than exponential at decreasing gate bias.
- Dielectric rupture through a high quality Si_3N_4 film at a field strength well below breakdown (as a result of hole injection and trapping from the adjacent pGaN region).

This lifetime equation is not simply borrowed from the body of standard reliability models developed for MOSFETs. Instead, it represents the first gate lifetime model, built up from the root physics of failure, specifically applicable to enhancement mode GaN transistors.

3.1.4. Gate Overvoltage Study

Gate overvoltage spikes during device turn-on transients are commonly observed in gallium nitride high electron mobility transistors (GaN HEMTs) under high-frequency, fast-switching conversion applications [8]. The magnitude of the gate overvoltage transients is primarily governed by the gate-loop inductance and the slew rate (V_{GS}/dt) which both are closely related to circuit design and PCB layout [10]. Therefore, it is critical to understand the gate overvoltage capability of GaN HEMTs as well as the associated lifetimes under various overvoltage stresses.

The projected lifetime results offer assurance that the failure rate is expected to be less than 1 part per million (ppm) for 25 years if the gate was biased less than the datasheet maximum limit at 6 $V_{GS,Max}$. This virtually zero failure rate is also consistent with EPC's field experience, where no gate failures have ever been identified despite very demanding applications in automotive, satellites, and advanced enterprise servers. This projected extremely low failure rate helps build confidence in overall gate reliability but does not provide a methodology to accurately estimate the overall lifetime when gate overvoltage spikes are present repetitively during switching.

In real-world applications, the common mission profile can be simplified and illustrated by Figure 3-4 [8,12]. Within each switching period (t_S), it mainly includes two portions which are labeled as overvoltage duration, t1, and bus voltage duration, t_2.

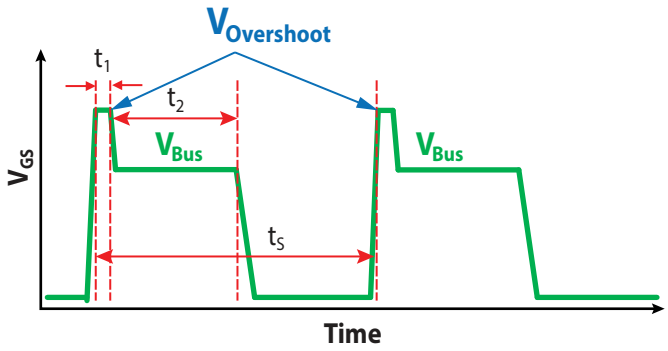


Figure 3-4: An illustration of a normal gate switching waveform in real-world applications. t_1 is the duration of gate overshoot in each period and t_2 is the nominal bus voltage bias duration within each switching period. t_S is the switching period that is dependent on the switching frequency.

By following the mathematical approach introduced in Section 2 using the durations shown Figure 3-4, Equation 3-2 is developed to estimate total lifetime by accounting for gate overshoot period and normal bus voltage period.

$$\frac{1}{T_{Total}} = \frac{a}{T_{VG_{Overshoot}}} + \frac{b}{T_{VG_{Bus}}} \quad \text{Eq. 3-2}$$

Another term, overshoot duty cycle, is introduced in Equation 3-3, where $DC_{overshoot}$ is the ratio between t1, gate overvoltage duration within each switching period, and the switching period, t_S that is inversely proportional to the switching frequency.

$$DC_{overshoot} = \frac{t_1}{t_s} \quad \text{Eq. 3-3}$$

To further demonstrate the model of Equations 3-2 and 3-3, two examples are provided in the following discussion, based on the data presented in Section 3.1.2. Assume the nominal bus voltage for EPC2212 is 5.5 V. The overvoltage is estimated to be 120% of the nominal bus voltage, which is calculated to be 6.6 V ($V_{GS,Max}$ = 6 V). The overshoot duty cycle is expected to be approximately 1% as defined by Equation 3-3 and Figure 3-4.

To simplify the calculation, it is assumed that the gate is operating 99% of the time at 5.5 V although there should always be another duty cycle involved in real applications. Therefore, adding the impact of the overshoot to the nominal drive condition, the EPC2212 GaN device lifetime is projected to be 1.64 x 10^9 seconds, or 51 years, for a 10 ppm failure rate (10 device failures per 1 million tested).

In another example, the GaN devices are used in a poorly designed circuit where the gate terminal sees a 7 V gate voltage spike during turn-on transient repetitively with the same 1% overshoot duty cycle. In this extreme example the bus voltage is still at 5.5 V for 99% of the time. After approximately 16 years, the failure rate is still expected to be only 100 ppm.

The test-to-fail approach was applied to GaN devices to investigate the gate reliability beyond the maximum datasheet limit. This work provides a comprehensive lifetime equation to account for the respective lifetimes under various gate bias conditions including overvoltage stress condition and nominal bus voltage bias condition. The projected lifetime based on 1% of gate overshoot duty cycle at 120% of V_{Bus} is expected to significantly exceed 25 years at a failure rate of 10 ppm. This result demonstrates excellent gate overvoltage reliability.

3.2 Drain Wear-Out

3.2.1 Introduction to Drain Wear-Out Mechanisms

The same test-to-fail methodology is adapted to investigate drain-related wear-out mechanism. One of the more common concerns among GaN transistor users is dynamic on-resistance, especially if their experiences are based on older generation products from various suppliers. This is a condition whereby the on-resistance of a transistor increases when the device is exposed to high drain-source voltage (V_{DS}). The dominant wear-out mechanism in GaN is uncovered and modeled from first principles, leading to a comprehensive lifetime equation to project dynamic $R_{DS(on)}$ shift with respect to various parameters, including voltage, temperature, frequency, and current etc. When overvoltage spikes are observed during switching applications, another duty cycle-based overvoltage specification is developed.

3.2.2 Physics-Based Dynamic $R_{DS(on)}$ and Lifetime Models

As shown in the Phase 15 report [1], the dominant mechanism causing on-resistance to increase is the trapping of electrons near the drain electrode. As the trapped charge accumulates, it depletes electrons from the two-dimensional electron gas (2DEG) in the ON state, leading to an increase in $R_{DS(on)}$.

Figure 3-5 is a magnified image of an EPC2016C GaN transistor showing thermal emissions in the 1–2 µm optical range. Emissions in this part of the spectrum are consistent with hot electrons and their location in the device is consistent with the location of the highest electric fields when the device is under drain-source bias.

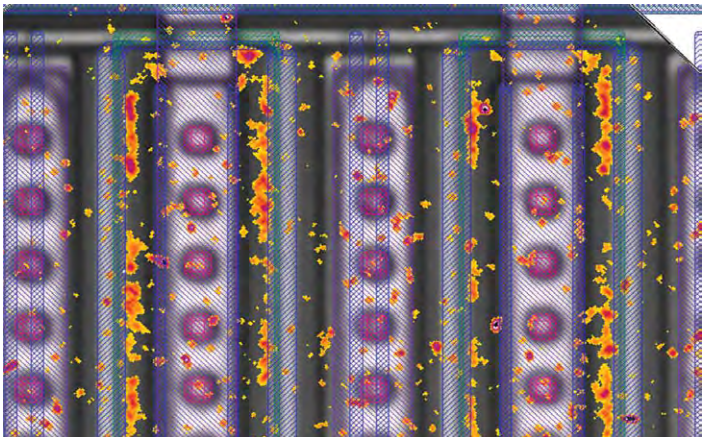


Figure 3-5: A magnified image of an EPC2016C GaN transistor showing light emission in the 1–2 µm wavelength short-wave infrared light range (SWIR) that is consistent with hot electrons. The SWIR emission (red-orange) has been overlaid on a regular (visible wavelength) microscope image and a semi-transparent image of the design photomask (purple).

Knowing that hot electrons in this region of the device are the source of trapped electrons, a better understanding of how to minimize the dynamic on-resistance can be achieved with improved designs and processes. By understanding the general behavior of hot electrons, their behavior over a wider range of stress conditions can be generalized.

Figure 3-6 shows how the $R_{DS(on)}$ of a fifth generation EPC2045 GaN transistor [13], designed with the knowledge that hot electron trapping is accelerated with peak electric fields near the drain, increases over time at various voltage stress levels and temperatures. On the top graph, the devices were tested at 25°C, at voltages from 60 V to 120 V (EPC2045 has a $V_{DS(max)}$ of 100 V). The horizontal axis shows time measured in minutes, with the right side ending at 10 years. The graph on the bottom shows the evolution of $R_{DS(on)}$ when biased at 120 V at different temperatures. The counter-intuitive result shows that the on-resistance increases faster at lower temperatures. This is consistent with hot-carrier injection because hot electrons travel further between scattering events at lower temperatures and therefore are accelerated to greater kinetic energies by a given electric field. The result is that the electrons scatter further with higher energies, reaching layers where they are more likely to become trapped. This suggests that traditional testing methods, where a device is tested at maximum voltage and temperature, may not be enough to determine the reliability of a device.

In the original publication of the results [5,9,14], the MTTF was found to be longer at 90°C than at either 35°C or 150°C, which was a mystery at the time. The results now can be better understood. As the device is heated under DC bias, the leakage current increases. However, the shorter mean free path of the hot carriers outweighs

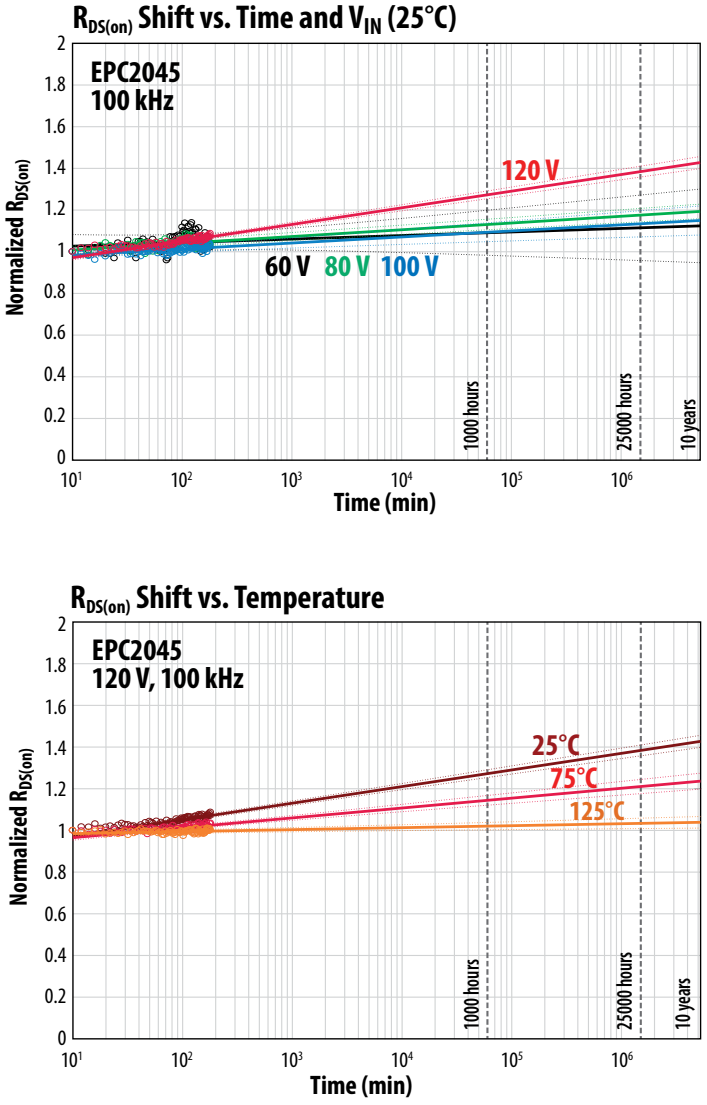


Figure 3-6: The $R_{DS(on)}$ of a fifth generation EPC2045 GaN transistor over time at various voltage stress levels and temperatures. On the left, the devices were tested at 25°C with voltages from 60 V to 120 V. The graph on the right shows the evolution of $R_{DS(on)}$ at 120 V at various temperatures.

the increase in available electrons such that the rate of $R_{DS(on)}$ increase falls from room temperature to 90°C. At temperatures above 90°C, leakage continues to grow and the rate of $R_{DS(on)}$ increase rises slightly.

When the applied drain bias is no greater than 120% of the $V_{DS,Max}$, indicating the trapped charge density is significantly smaller than the 2DEG carrier concentration, the model for $R_{DS(on)}$ growth is shown in Equation 3-4.

Eq. 3-4

$$\frac{\Delta R}{R} = a + b\log\left(1+\exp\left(\frac{V_{DS}-V_{FD}}{\alpha}\right)\right)\sqrt{T}\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\log(t)$$

Independent Variables:

V_{DS} = Drain voltage (V)

T = Device temperature (K)

t = Time (min)

Parameters:

a = 0.00 (unitless)

b = 2.0E-5 ($K^{-1/2}$)

$\hbar\omega_{LO}$ = 92 meV

V_{FD} = 100 V (appropriate for Gen5 100 V products only)

α = 10 (V)

k = Boltzmann constant=0.0862 meV/K

Many customers require lifetime estimates under specific use conditions to fulfill certain quality or reliability requirements. By defining the lifetime (under hard-switching conditions) as the time <t> at which $R_{DS(on)}$ will rise 20% from its initial value, Equation 3-4 can be inverted in a straightforward manner to obtain the time to failure

$$\langle t \rangle = \exp\left[\frac{(0.2-a)}{b\log\left(1+\exp\left(\frac{V_{DS}-V_{FD}}{\alpha}\right)\right)\sqrt{T}\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)}\right] (\text{min}) \quad \text{Eq. 3-5}$$

This equation gives the expected MTTF under hard-switching conditions as a function of operating voltage and temperature. Typically, worst case values (highest voltage, lowest temperature) are used to provide a lower bound. As before, the lifetime will be in units of minutes. Other definitions of lifetime can be applied and extracted from Equation 3-4 as well.

3.2.3. Effect of Switching Frequency and Switching Current

In the analysis so far, the effects of switching frequency (f) and switch current (I) on the $R_{DS(on)}$ growth characteristics have been ignored. The current directly impacts the number of electrons injected into the high field region during the hard-switching transition, and therefore has a linear effect on the hot carrier density. Likewise, the switching frequency determines the number of hot carrier pulses seen at the drain in a given time interval, and therefore also has a linear effect on the surface trapping rate.

By assuming that the surface trapping rate is linearly proportional to both frequency (f) and current (I), the effects of f and I are included in Equation 3-6, where a simple scaling term is derived to relate the $R_{DS(on)}$ growth in one switching condition (f_1, I_1) to another (f_2, I_2).

$$R(t; f_2, I_2) = R(t; f_1, I_1) + b\left(\log\left(\frac{f_2}{f_1}\right) + \log\left(\frac{I_2}{I_1}\right)\right) \quad \text{Eq. 3-6}$$

Mathematically, the effect of changing the switching frequency or current is to simply offset the $R_{DS(on)}$ growth curve vertically by a small amount. The offset depends on the logarithm of f and I, and therefore has a fundamentally weak dependence on these variables. Furthermore, the offset depends on the overall slope b of the log(t) growth characteristic. Therefore, if the FET is operated under conditions with low $R_{DS(on)}$ rise (low slope b), the effect of changing frequency or current will be negligible.

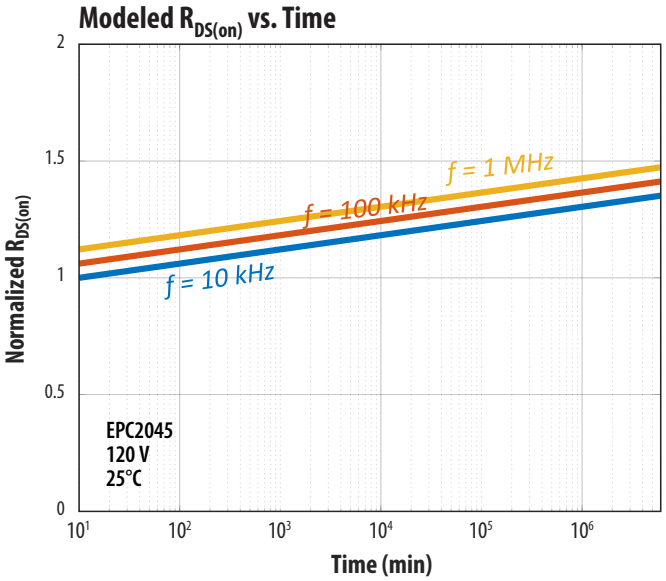


Figure 3-7: Modeled $R_{DS(on)}$ vs. Time at three different switching frequencies, covering two orders of magnitude. Note that the effect of frequency change is a small vertical offset in the growth characteristic. The same offset would occur at different switch currents.

I, and therefore has a fundamentally weak dependence on these variables. Furthermore, the offset depends on the overall slope b of the log(t) growth characteristic. Therefore, if the FET is operated under conditions with low $R_{DS(on)}$ rise (low slope b), the effect of changing frequency or current will be negligible.

Figure 3-7 compares the modeled $R_{DS(on)}$ vs. time for an EPC2045 at three different switching frequencies, from 10 kHz to 1 MHz. Note that the curves are simply offset from each other vertically. The same would be true had we compared different switch currents. Because the offset changes as the logarithm of f (or I), even a 10x increase in switching frequency (or current) would be difficult to observe experimentally owing to ±10% noise in the measurement and projection.

3.2.4. Impact of Higher Stress Voltages

In the case where the amount of trapped charge approaches the number of electrons available in the 2DEG (the surface trapped charges (Q_S) approaches the built-in 2DEG piezoelectric charge (Q_P)), the simplifying assumption used to develop Equation 3-4 is no longer valid. This situation could occur when devices are taken to voltages well above their design limits. Figure 3-8 shows results for EPC2045 devices tested up to 150 V at 75°C and 125°C. Note how the straight-line extrapolation that would occur with a simple log(time) dependence is no longer applicable. By removing the simplified assumption that only a small fraction of Q_P is trapped and transform into Q_S, the result shown in Equation 3-7 is obtained.

Calculating Equation 3-7 using the expanded list of parameters yields the solid lines in Figure 3-8, providing further evidence of the validity and applicability of this physics-based model.

$$\frac{\Delta R}{R} = a_1\left[\frac{a_2\Psi\, log\,(1+a_3 t/\Psi)}{1-a_2\Psi\, log\,(1+a_3 t/\Psi)}\right]$$

where:

$$a_1 \equiv \frac{C}{Q_P} \qquad a_2 \equiv \frac{1}{Q_P} \qquad a_3 \equiv B \qquad \text{Eq. 3-7}$$

with the following expanded list of parameters:

- a_1 = 0.6 (unitless)
- a_2 = b/a_1 (where b = 2.0E-5 $K^{-1/2}$ from [5,9])
- a_3 = 1000 ($K^{1/2}$ min^{-1})
- b = 2.0E-5 ($K^{-1/2}$)
- $\hbar\omega_{L0}$ = 92 meV
- V_{FD} = 100 V (appropriate for Gen5 100 V products only)
- α = 10 (V)
- T = Device temperature (K)
- t = Time (min)

3.2.5 200 V Model

A similar analysis was developed for 200 V GaN transistors. The resultant variables are as follows:

- a_1 = 0.6 (unitless)
- a_2 = 2.8·b/a_1 (where b = 2.0E-5 $K^{-1/2}$ from [7])
- a_3 = 1000 ($K^{1/2}$ min^{-1})
- b = 2.0E-5 ($K^{-1/2}$)
- $\hbar\omega_{L0}$ = 92 meV
- V_{FD} = 210 V (appropriate for Gen5 200 V products only)
- α = 25 (V) (appropriate for Gen5 200 V products only)
- T = Device temperature (K)
- t = Time (min)

Figure 3-9 compares this model to measurements of 200 V devices. On the left is the normalized $R_{DS(on)}$ for the fifth-generation, 200 V rated EPC2215 at three voltages. The highest voltage, 280 V, is 40% above the maximum rating. On the right are measurements compared with the model at two different temperature and the maximum rated voltage.

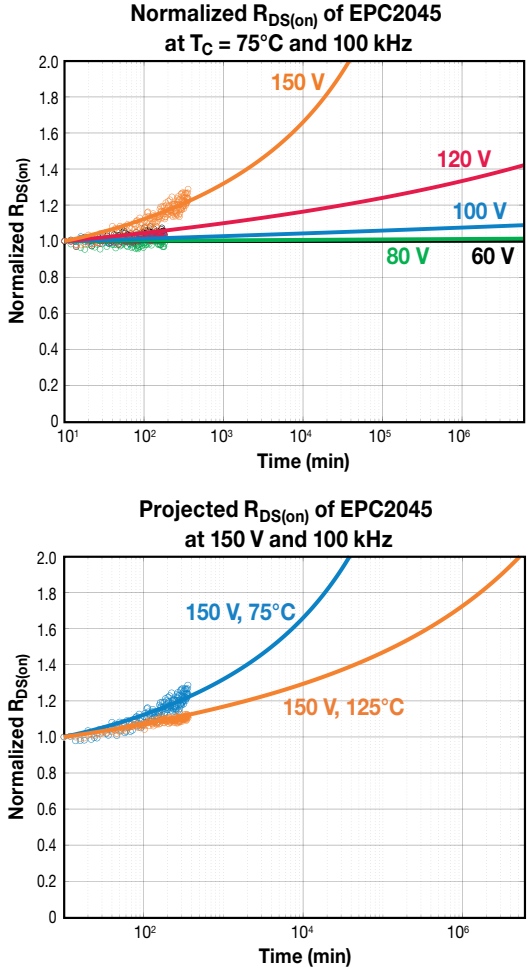


Figure 3-8: 100 V EPC2045 devices in hard-switching circuit at various voltages up to 150% of design rating (top), and at two different temperatures, also at 150% of design rating (bottom). The solid lines are the model predictions, and the dots represent measurement points.

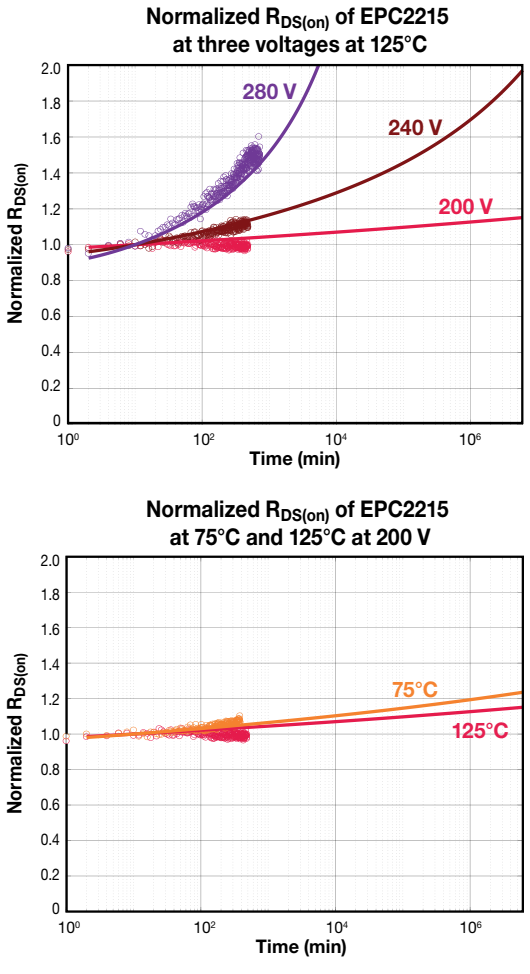


Figure 3-9: (Top) 200 V EPC2215 normalized $R_{DS(on)}$ at three voltages. Note that 280 V is 40% above the maximum rated voltage. (Bottom) EPC2215 at 75°C and 125°C and 200 V. The solid lines are the model results using variables for 200 V devices, and the dots are actual measurements.

3.2.6. Drain Overvoltage Specification

Transient drain voltage overshoot is commonly observed in gallium nitride-based converters due to high slew rate and fast switching applications. A survey of transient overvoltage specification from a suite of GaN suppliers was conducted by JEDEC JC-70 committee and presented in JEP186 [15]. Most of the transient overvoltage specifications describe it as a device robustness indicator. In addition, many of them consider drain voltage overshoot as a single rare event or atypical occurrence. Hence, it is challenging for application engineers to effectively implement these specifications into their designs. Therefore, an application driven, and user-friendly repetitive transient off-state drain overvoltage specification on datasheets is important for the general adoption of GaN technology because of the absence of avalanche mechanisms in GaN HEMTs.

A resistive-load hard switching system (also known as "fast dR") [1,5,9,14] was deployed to study dynamic $R_{DS(on)}$ shift under cumulative drain overshoot stress, where this system operates at 100 kHz, 85% of the time reverse-biasing the GaN device under test (DUT) at the specified off-state drain voltage. When determining time of failure, 20% of $R_{DS(on)}$ shift compared to the initial $R_{DS(on)}$ value after a projected 25 years of stress is used as the failure criteria. Equation 3-4 is used to extrapolate the time-of-failure when the in-situ monitored $R_{DS(on)}$ shifts more than 20% to its initial value (R_0). This approach is more stringent than the typical datasheet maximum $R_{DS(on)}$ limit.

A suite of 100 V fifth generation GaN products were tested by the fast dR system at 120% of $V_{DS,Max}$ (120 V) and 75°C junction temperature, a common mission temperature. EPC2045 was the first 100 V rated GaN product that was launched from the fifth-generation 100 V product family. EPC2045 was first subjected to testing under such accelerated conditions. Figure 3-10 shows the testing results, where the DUT is projected to exceed the 20% $R_{DS(on)}$ shift limit at approximately 2 x 10^5 minutes by considering a 90% upper bound confidence level. Lifetime extrapolation is based upon the logarithmic time relation.

By multiplying by 85%, it yields 1.7 x 10^5 minutes, representing the total lifetime when the DUT is off-state biased continuously under 120 V and 75°C. When comparing with 25 years of expected overall lifetime, equivalent of 1.3 x 10^7 minutes, 1.7 x 10^5 minutes translates to approximately 1.3% of total lifespan. To add more margin, we rounded to 1% of 25 years. Now a total lifetime-based overvoltage specification of 1.3 x 10^5 minutes is developed.

To further validate this total time-based specification, the same testing conditions were applied to newer 100 V rated GaN products including EPC2218, EPC2071, EPC2302, and EPC2204. Figure 3-11 summarizes the testing results of the listed products, where they are all projected to outperform the 1.3 x 10^5 minutes of lifetime.

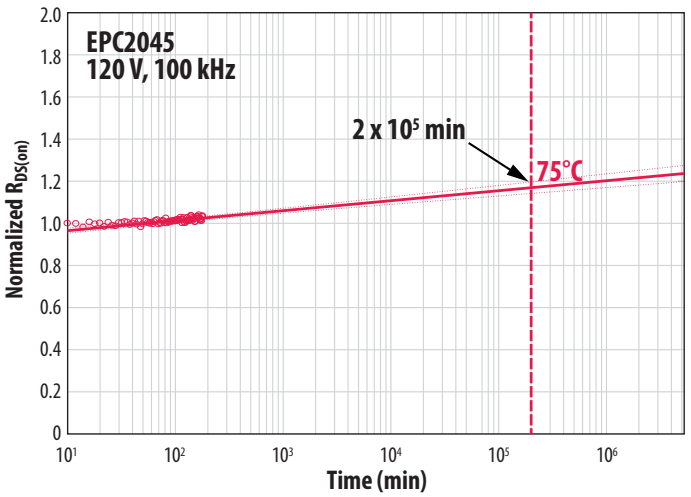


Figure 3-10: Evolution of $R_{DS(on)}$ of a representative EPC2045 device, a fifth-generation 100 V rated GaN transistor, tested at 120 V and 75°C. It is projected to exceed 20% $R_{DS(on)}$ shift at 2 x 10^5 minutes by considering 90% of upper bound confidence level.

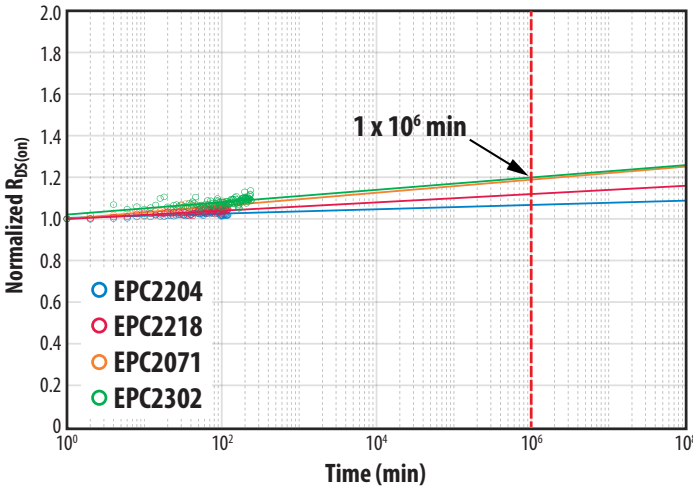


Figure 3-11: Evolution of $R_{DS(on)}$ of representative EPC2204, EPC2218, EPC2071, and EPC2302 GaN transistors, rated at 100 V and tested at 120 V and 75°C. They are projected to have less than 20% $R_{DS(on)}$ shift at a minimum of 1 x 10^6 minutes, significantly exceeding the 2 x 10^5 minutes lifetime based on EPC2045.

This total time-based specification can be scaled to a shorter duration that occurs repetitively within each switching cycle. Therefore, another way to specify this repetitive rating is to calculate the ratio of overvoltage duration of each cycle over the switching period, which is the 1% scaling factor that was initially discussed. This is equivalent to calculating the duty cycle of the overvoltage spike.

For instance, if a converter operates at 100 kHz, equivalent of 10 µs per switching period, it suggests that the GaN devices should withstand a repetitive 120 V overvoltage spike with a 100 ns duration in each switching cycle over 25 years of lifetime. This mathematical relation is demonstrated in Equation 3-8 and further illustrated in Figure 3-12.

Eq. 3-8

$$Overshoot\ duty\ cycle = \frac{120\%\ Overvoltage\ Duration\ at\ 75°C\ (T_O)}{Switching\ Period\ (T_S)} \leq 1\%$$

where T_O is the overvoltage duration within each switching period and T_S is the switching period.

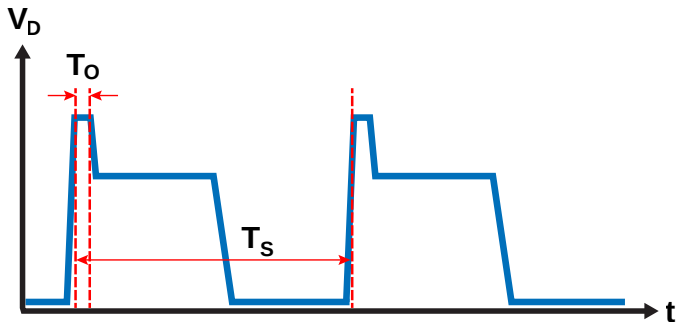


Figure 3-12: Illustration of the 1% overshoot duty cycle overvoltage specification. 1% is the ratio between T_O (overvoltage duration) and TS (one switching period).

To verify this newly proposed overvoltage specification method, an unclamped inducive switching (UIS) circuit was developed [16,17]. Figure 3-13 shows the resulting overvoltage pulse that is generated by UIS.

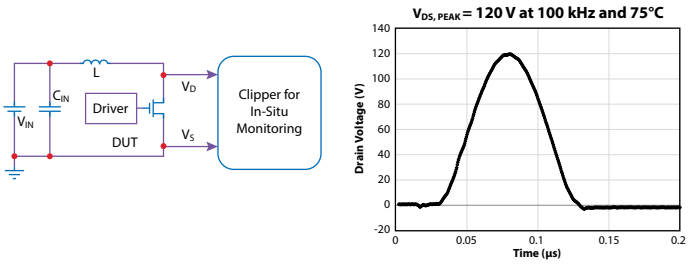


Figure 3-13: Simplified schematic of the unclamped inductive switching circuit and the resulting overvoltage pulse with $V_{DS,Peak}$ of 120 V under 100 kHz operating frequency.

A number of 100 V rated GaN transistors from different wafer lots are stressed by a 120 $V_{DS,Peak}$ overvoltage spike at 100 kHz operation frequency and 75°C junction temperature. Figure 3-14 shows that representative EPC2218 devices from three different wafer lots were tested to billions of switching cycles showing very small dynamic $R_{DS(on)}$ shift.

The same physics-based lifetime model based on hot carrier trapping was applied to project the lifetime under such drain overvoltage stresses. The projection demonstrates the excellent robustness of GaN devices under 120% overvoltage stress over long-term continuous operation. At each switching cycle, the duration exceeding 100 $V_{DS,Max}$ is approximately 25 ns, lower than the 120 V peak overshoot voltage. At the end of 8 x 10^8 seconds (25 years), which equates to 8 x 10^{13} total pulses by multiplying with 100 kHz frequency, none of the DUTs surpassed the 20% $R_{DS(on)}$ shift failure criteria. Multiplying 25 ns by 8 x 10^{13} pulses gives 2 x 10^5 minutes, which is close to the estimated total lifetime of 1.3 x 10^5 minutes. The slight difference can be explained by the fact that the DUTs only reach the 120 V peak voltage for a very short portion of each pulse. The voltage waveform shown in Figure 3-13 is more representative of real time circuit applications.

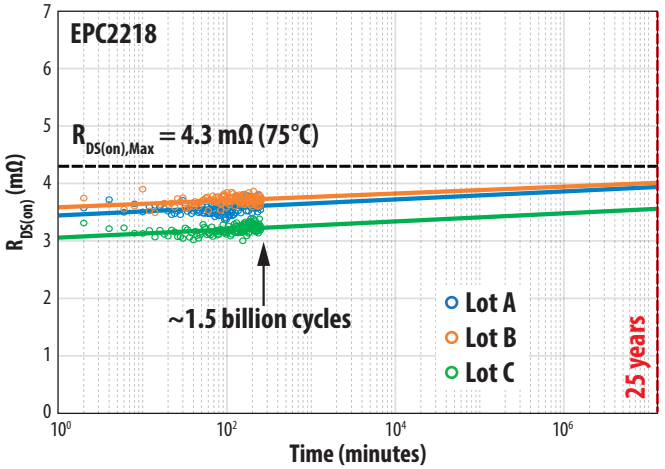


Figure 3-14: Evolution of dynamic $R_{DS(on)}$ of a representative EPC2218 DUTs from three different wafer lots under 120 $V_{DS,Peak}$ and 75°C UIS testing for more than 1.5 billion cycles.

EPC2302, a representative power quad flat no-lead (PQFN) packaged 100 V rated GaN transistor was also tested in UIS at 120 $V_{DS,Peak}$ for more than 10 billion switching cycles. The projected lifetime showed extreme robustness of GaN devices under such overvoltage stress condition, shown in Figure 3-15. This further validates the proposed overvoltage specification.

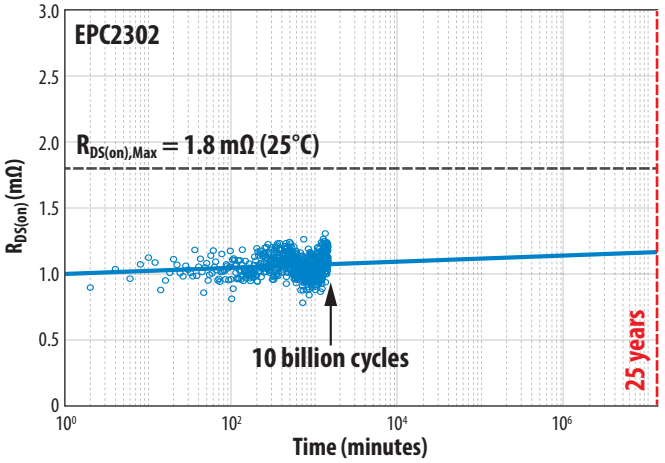


Figure 3-15: Evolution of dynamic $R_{DS(on)}$ of a representative EPC2302 DUT under 120 $V_{DS,Peak}$ UIS testing for approximately 10 billion switching cycles.

A repetitive drain overvoltage specification is proposed and validated by resistive load hard switching and unclamped inductive switching testing circuits. This duty cycle-based specification offers a more quantitative and easy-to-implement guideline for application engineers to design GaN devices. This work also demonstrates the extreme overvoltage robustness of GaN HEMTs.

3.2.7. Conclusions for Physics-Based Dynamic $R_{DS(on)}$ Model

EPC has developed a first principles physics-based model to explain $R_{DS(on)}$ rise in GaN transistors under hard-switching conditions. The model is predicated on the assumption that hot electrons are injected over a surface potential into the conduction band of the surface dielectric. Once inside, the electrons quickly fall into deep mid-gap states, where they are assumed to be trapped permanently (no de-trapping). Hot electrons are created during the switching transition, where the transient combination of high injection current and high fields leads to a hot carrier energy distribution with long tails into the high energy regime.

This model predicts the following observations:

- Small $R_{DS(on)}$ growth with time
- The slope of $R_{DS(on)}$ over time has a negative temperature coefficient (i.e., lower slope as temperature rises).
- Switching frequency does not affect the slope but causes a small vertical offset.
- Switching current does not affect the slope.

The time dependence results from a rapidly self-quenching charge trapping dynamic that involves two intertwined effects: (1) a hot electron energy distribution that is exponential in energy; and (2) an accumulating surface charge Q_S that steadily raises the barrier for electron injection into the dielectric [9]. The combination of these effects leads to a trapping rate that becomes exponentially slower as charge accumulates, leading to a slow time dependence. As the number of trapped charges approaches the number of available electrons in the 2DEG, the $R_{DS(on)}$ appears to climb faster than a straight log(time) dependence. The trapping mechanism, however, continues to follow a true log(time) dependence.

The negative temperature dependence results from the effect of LO-phonon scattering on the hot carrier energy distribution. At lower temperature, decreased scattering improves the mean free path, allowing electrons to gain higher energy in an electric field.

Key parameters in the mathematical model were fit to measured results for the EPC2045 across a range of drain voltages and temperatures. The model allows users to project long-term $R_{DS(on)}$ growth as a function of four key input variables: drain voltage, temperature, switching frequency, and switching current. The model was adapted to provide a simple MTTF equation, allowing users to predict lifetime under arbitrary conditions.

3.3. Current Density Wear-out

3.3.1. Introduction to Current Density Wear-out Mechanisms

Thermal limits can be of concern for GaN devices when high current and high drain-source voltage occur simultaneously. Extensive robustness testing was conducted, and the results verified the validity of safe operating area specified by the datasheet. For certain applications, the capability of withstanding short circuit fault conditions is a must. Therefore, short circuit testing was performed, where GaN demonstrated excellent robustness under such extreme stress conditions. When the devices are exposed to continuous high current at elevated temperatures, electromigration (EM) robustness becomes a frequently asked question by customers. Accelerated EM testing was conducted on power quad-flat no-leads (PQFN) devices, demonstrating excellent robustness against EM.

3.3.2. Safe Operating Area

Safe operating area (SOA) testing exposes the GaN transistor to simultaneous high current (I_D) and high voltage (V_{DS}) for a specified pulse duration. The primary purpose is to verify the transistor can be operated without failure at every point (I_D, V_{DS}) within the datasheet SOA graph. It is also used to probe the safety margins by testing to fail outside the safe zone. During SOA tests, the high-power dissipation within the die leads to a rapid rise in junction temperature and the formation of strong thermal gradients. For sufficiently high power or pulse duration, the device simply overheats and fails catastrophically. This is known as thermal overload failure.

In Si MOSFETs, another failure mechanism known as secondary breakdown (or Spirito effect [18]) has been observed in SOA testing. This failure mode, which occurs at high V_D and low I_D, is caused by unstable feedback between junction temperature and threshold V_{TH}. As the junction temperature rises during a pulse, V_{TH} drops, which can cause local current to rise. The rising current, in turn, causes temperature to rise faster, thereby completing a positive feedback loop that leads to thermal runaway and ultimate failure. A goal of this study is to determine if the Spirito effect exists in GaN transistors.

For DC, or long-duration pulses, the SOA capability of the transistor is highly dependent on the heatsinking of the device. This can present a huge technical challenge to assess the true SOA capability, often requiring specialty water-cooled heatsinks. However, for short pulses (< 1 ms), the heatsinking does not impact SOA performance. This is because on short timescales the heat generated in the junction does not have sufficient time to diffuse to any external heatsink. Instead, all the electrical power is converted to raising the temperature (thermal capacitance) of the GaN film and nearby silicon substrate. As a result of these considerations, SOA tests were conducted at two pulse durations: 1 ms and 100 µs.

Figure 3-16 shows the SOA data of 200 V EPC2034C. In this plot, individual pulse tests are represented by points in (I_D, V_{DS}) space. These points are overlaid on the datasheet SOA graph. Data for both 100 µs and 1 ms pulses data are shown together. Green dots correspond to 100 µs pulses in which a part passed, whereas red dots indicate where a part failed. A broad area of the SOA was interrogated without any failures (all green dots), ranging from low V_{DS} all the way to V_{DSmax} (200 V). All failures (red dots) occurred outside the SOA, indicated by the green line in the datasheet graph. The same applies to 1 ms pulse data (purple and red triangles); all failures occurred outside of the datasheet SOA.

Figure 3-17 provides SOA data for three more parts, AEC EPC2212 (4th generation automotive 100 V), EPC2045 (5th generation 100 V), and EPC2014C (4th generation 40 V). In all cases, the datasheet safe operating area has been interrogated without failures, and all failures occur outside of SOA limits, often well outside the limits.

The datasheet SOA graph is generated with finite element analysis, using a thermal model of the device including all relevant layers along with their heat conductivity and heat capacity. Based on transient simulations, the SOA limits are determined by a simple criterion: for a given pulse duration, the power dissipation must be such that the junction temperature does not exceed 150°C before the end of the pulse. This criterion results in limits based on constant power, denoted by the 45° green (100 µs) and purple (1 ms) lines in the SOA graph. This approach leads to a datasheet graph that defines a conservative safe operating zone, as evidenced by the extensive test data in this study. In power MOSFETs, the same constant power approach leads to an overestimate of capability in the high voltage regime, where failure occurs prematurely due to thermal instability (Spirito effect).

While the exact physics of failure is yet to be determined, the main outcome of this study is clear – GaN transistors will not fail when operated within their datasheet SOA.

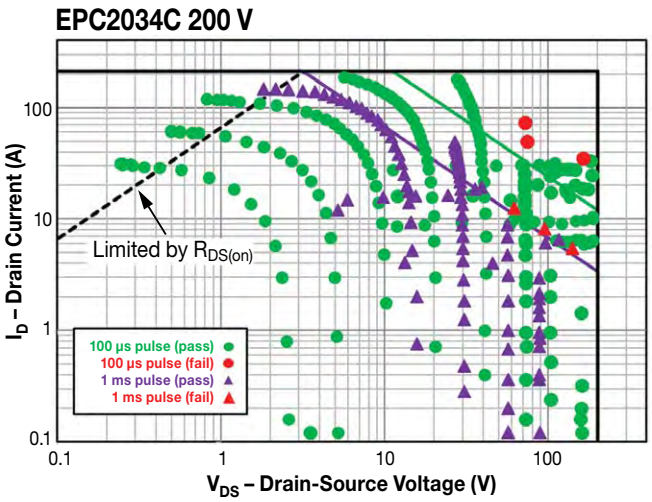


Figure 3-16: EPC2034C SOA plot. The "Limited by $R_{DS(on)}$" line is based on datasheet maximum specification for $R_{DS(on)}$ at 150°C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that all failures occur outside the datasheet SOA region.

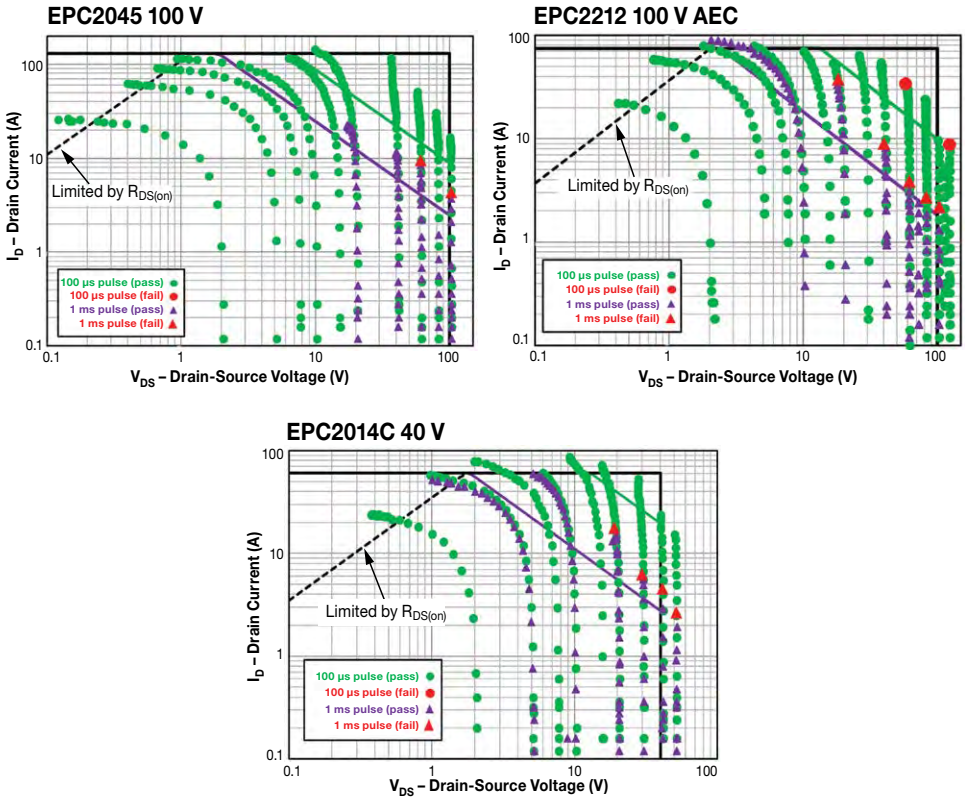


Figure 3-17: SOA results for EPC2045, EPC2212, EPC2014C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles.

3.3.3. Short-Circuit Robustness Testing

Short circuit robustness refers to the ability of a FET to withstand unintentional fault conditions that may occur in an application while in the ON (conducting) state. In such an event, the device will experience the full bus voltage combined with a current that is limited only by the inherent saturation current of the transistor and the circuit parasitic resistance, which varies with the application and location of the fault. If the short-circuit state is not quenched by protection circuitry, the extreme power

dissipation will ultimately lead to thermal failure of the transistor. The goal of short-circuit testing is to quantify the "withstand time" the part can survive under these conditions.

Typical protection circuits (e.g., de-saturation protection for IGBT gate drivers) can detect and react to over-current conditions in 2–3 µs. It is therefore desirable if the GaN transistor can withstand unclamped short-circuit conditions for about 5 µs or longer.

The two main test circuits used for short-circuit robustness evaluation are described in [28]. They are:

- Hard-switched fault (HSF): gate is switched ON (and OFF) with drain voltage applied.
- Fault under load (FUL): drain voltage is switched ON while gate is ON.

For this study, devices were tested in both fault modes and no significant differences in the withstand time were found. Therefore, the focus will be on FUL results for the remainder of this discussion. However, it is important to note that from HSF testing, GaN transistors did not exhibit any latching or loss of gate control that can occur in silicon based IGBTs [69]. This result was expected given the lack of parasitic bipolar structures with the GaN devices. Until the time the transistors fail catastrophically, the short circuit can be fully quenched by switching the gate LOW, an advantageous feature for protection circuitry design.

Two representative GaN transistors were tested:

1. EPC2203 (80 V): 4th generation automotive grade (AEC) device
2. EPC2051 (100 V): 5th generation device

These devices were chosen because they are the smallest in their product families. This simplified the testing owing to the high currents required for short-circuit evaluation. However, based on simple thermal scaling arguments, the withstand time is expected to be identical for other in-family devices. EPC2203 results cover EPC2202, EPC2206, EPC2201 and EPC2212; EPC2051 covers EPC2045 and EPC2053.

Figure 3-18 shows fault-under-load data on EPC2203 for a series of increasing drain voltages. With V_{GS} at 6 V (the datasheet maximum), and a 10 µs drain pulse, the device did not fail all the way up to V_{DS} of 60 V. Under these conditions, over 1.5 kW is dissipated in a 0.9 x 0.9 mm die. At the higher V_{DS}, the current is seen to decay over time during the pulse. This is a result of rising junction temperature within the device and does not signify any permanent degradation.

Using a longer pulse duration (25 µs), the parts eventually fail from thermal overload. Representative waveforms are shown in Figure 3-19. The time of failure is marked by the abrupt sharp rise in drain current. After this event, the devices are permanently damaged. The withstand time is measured from the beginning of the pulse to the time of failure.

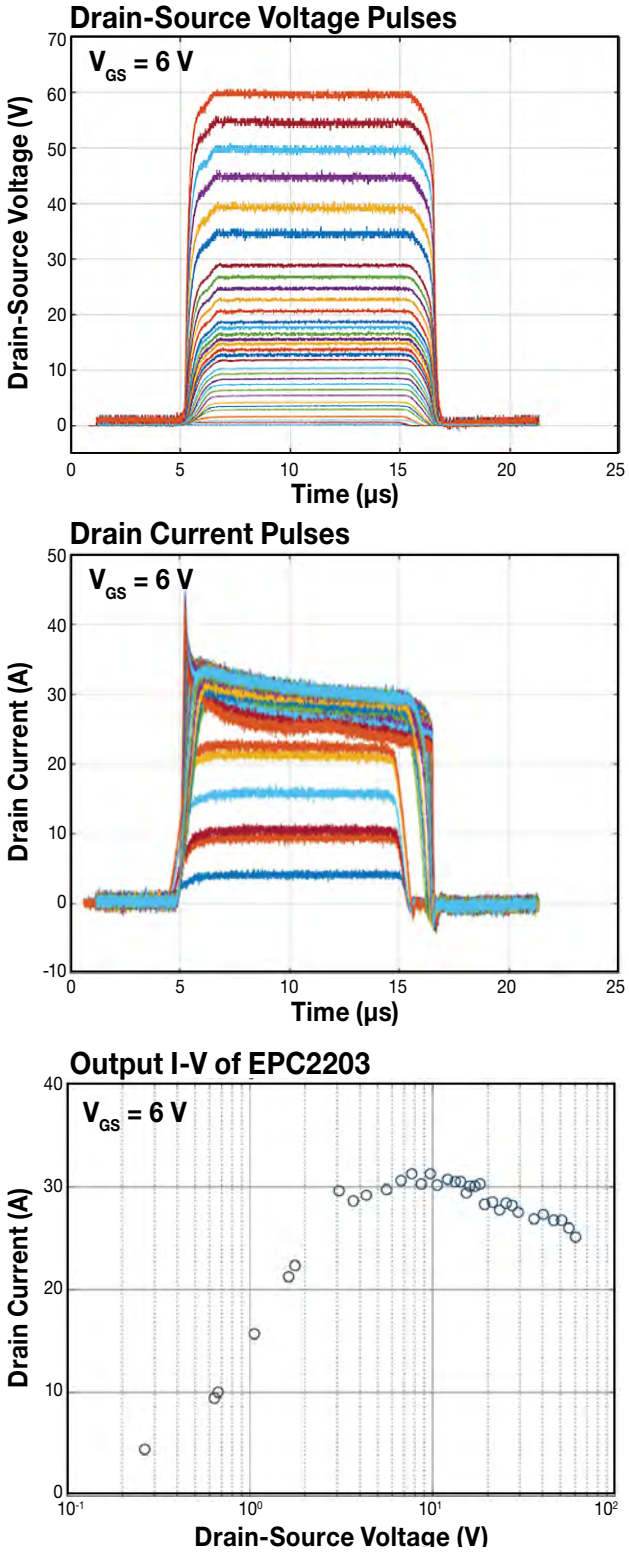


Figure 3-18: EPC2203 fault under load test (FUL) waveforms for a series of increasing drain voltages. Drain pulse is 10 µs and V_{GS} = 6 V. The device did not fail for this pulse width. In the V_{DS} vs. time plot (top), V_{DS} is Kelvin-sensed directly at the device terminals. In the IDS vs. time plot (center), it is noted that I_{DS} decreases over time due to self-heating. Resulting output curve for this test sequence (bottom). Drain current is reported as the average current during the pulse. Drain current rolls over in the saturation region owing to device heating at higher V_{DS}.

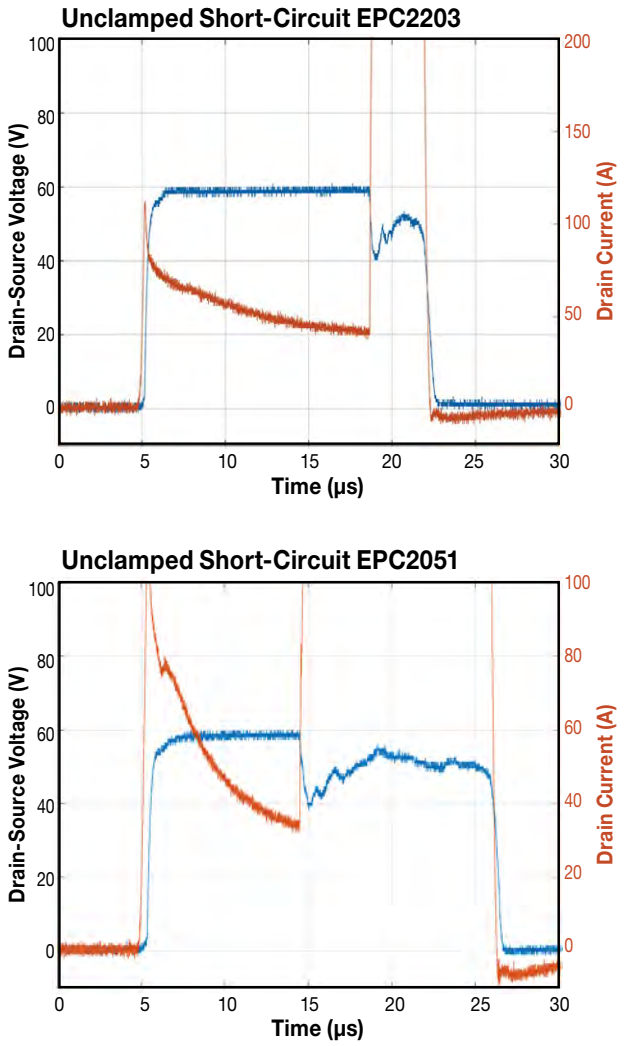


Figure 3-19: Fault-under-load test waveforms for a typical EPC2203 (top) and EPC2051 (bottom) at V_{DS} = 60 V, V_{GS} = 6 V, and a 25 µs drain pulse. The abrupt rise in drain current marks the time of catastrophic thermal failure.

To gather statistics on the withstand time, cohorts of eight parts were tested to failure using this approach. Table 3-1 summarizes the results. EPC2203 was tested at both 5 V (recommended gate drive) and 6 V ($V_{GS(max)}$), with mean withstand time of 20 µs and 13 µs, respectively. Note that the device survives less time at 6 V because of the higher saturation current. EPC2051 exhibited a slightly lower time-to-fail (9.3 µs) compared with the EPC2203 at 6 V. This is expected because of the more aggressive scaling and current density of 5th generation products. However, in all cases, the withstand time is comfortably long enough for most short-circuit protection circuits to respond and prevent device failure. Furthermore, the withstand time showed small part-to-part variability.

The lower rows in Table 3-1 provide pulse power and energy relative to die size. To gain insight into the relationship between these quantities and the time to failure, time-dependent heat transfer was simulated to determine the rise in junction temperature ΔT_J during the short-circuit pulse. The results are shown in Figure 3-20.

Short-circuit pulse V_{DS} = 60 V	**EPC2203 (Gen 4)**		**EPC2051 (Gen 5)**	
	V_{GS} = 6 V	V_{GS} = 5 V	V_{GS} = 6 V	V_{GS} = 5 V
Mean TTF (µs)	13.1	20.0	9.33	21.87
Std. dev. (µs)	0.78	0.37	0.21	2.95
Min. TTF (µs)	12.1	19.6	9.08	18.53
Avg pulse power (kW)	1.764	1.4	3.03	2.03
Energy (mJ)	23.83	27.6	27.71	42.49
Die area (mm²)	0.9025		1.105	
Avg power/area (kW/mm²)	1.95	1.55	2.74	1.84
Energy/area (mJ/mm²)	26.4	30.59	25.08	38.46

Table 3-1: Short-circuit withstand time statistics for EPC2203 and EPC2051

Note: Statistics derived from eight devices in each condition. Withstand times are tightly distributed around mean value. Average pulse power and energy correspond to a typical part within the population.

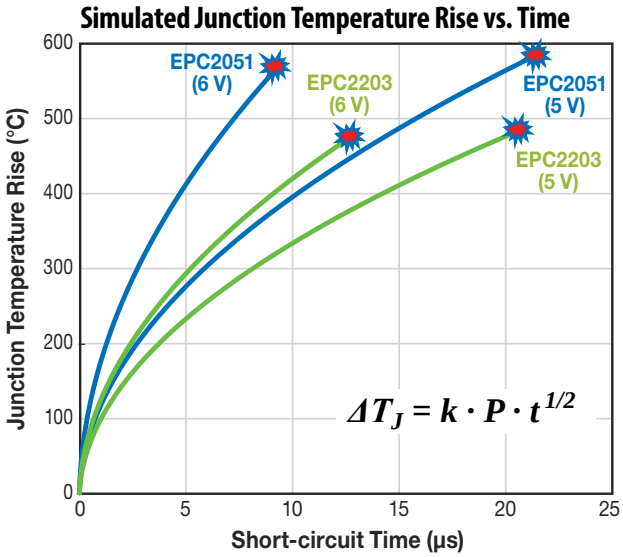


Figure 3-20: Simulated junction temperature rise versus time during the short-circuit pulses for both EPC2051 and EPC2203 at both 5 and 6 V_{GS}. Measured failure times are indicated by red markers. Note that EPC2203 fails catastrophically at a ΔT_J of around 475°C, whereas EPC2051 fails around 575°C. The simulated ΔT_J is well fit by a simple square root dependence on time (heat diffusion), as shown in the equation. P denotes the average power per unit area, and k = 6.73 x 10^{-5} K m^2/W $s^{1/2}$.

The intense power density during the pulse leads to rapid heating in the GaN layer and nearby silicon substrate. Because the pulse is short and heat transfer is relatively slow, only a small thickness of semiconductor (< ~100 µm in depth) can help to absorb the energy. The temperature grows as the square root of time (characteristic of heat diffusion), and linearly with the pulse power. As can be seen in Figure 3-20, for EPC2203, both the 5 V and 6 V conditions fail at the same junction temperature rise of ~475°C.

The same is true for EPC2051, where both conditions fail at the same ΔT_J of ~575°C. Three key conclusions stem from these results:

1. For a given device, the time to failure is inversely proportional to the power dissipation squared (P^{-2}). This applies for short-circuit and SOA pulses of duration < ~1 ms.
2. The intrinsic failure mode resulting from high power pulses is directly linked to the junction temperature exceeding a certain critical value.
3. Wide bandgap eGaN devices can survive junction temperatures (> 400°C) that are totally inaccessible to silicon devices owing to free-carrier thermal runaway.

To establish whether devices could survive these extreme conditions repetitively, several parts were subjected to over 500,000 cycles under short-circuit conditions that caused device currents about twice the maximum rated pulse current listed on their datasheets. In the test setup, gate bias of either 5 or 6 V_{GS} was applied to the device under test (DUT). Drain bias was set at 10 V_{DC} and a 60 mF capacitor was connected across the drain supply. A low $R_{DS(on)}$ high-side transistor in series with the DUT controlled the otherwise unlimited flow of current. The control transistor was then pulsed with 5 µs pulses at 1 Hz to give the channel time to re-equilibrate. Table 3-2 shows the various types of devices tested, their datasheet rating for maximum pulsed current, and the amount of short-circuit current that pulsed through the device during each cycle at the start of the test.

Device	Type	Datasheet pulsed (A)	V_{GS}	Mean (A)	Sigma (A)
EPC2203	80 V AEC Gen4	17	5	35	2.4
			6	43	2.5
EPC2212	100 V AEC Gen4	75	5	124	2.1
			6	160	3.5
EPC2051	100 V Gen5	37	5	68	1.0
			6	87	1.3
EPC2052	100 V Gen5	74	5	147	1.6
			6	163	2.2
EPC2207	200 V Gen5	54	5	99	4.7
			6	132	5.0

Table 3-2: Devices tested under extreme pulsed short-circuit current, typically twice the maximum datasheet limit.

Table 3-3 shows the various key device parameters for EPC2051, the same part number as used in Table 3-2 and in Figure 3-20. Even under these extreme conditions of 500,000 85 A pulses that are more than twice the datasheet maximum ratings, all electrical characteristics remained within datasheet specifications. There was, however, a small reduction in the amount of short circuit current "consumed" by the DUT over time, consistent with the small increase in V_{TH}. After this 500,000-pulse sequence, this part underwent an unbiased 10 minute anneal at 175°C. As can be seen in the right-hand column of Table 3-3, the electrical parameters and short-circuit current recovered to near their values before being subjected to repetitive pulse stresses. This recovery indicates that no permanent damage occurred from repetitive high-current pulses.

EPC2051	t = 0	100 k pulses	500 k pulses	Post 10 min. 175°C Anneal
V_{TH} (V)	1.8	2	2.1	1.8
I_{GSS} (µA)	11	33	55	23
I_{DSS} (µA)	7	5.5	5.1	5.6
$R_{DS(on)}$ (mΩ)	22	22.3	22.3	22
$I_{short\ circuit}$	84	77	74	82

Table 3-3: Key device parameters for EPC2051 at the start of pulse testing, after 100 k pulses, after 500 k pulses, and after a 175°C, 10 minute anneal. Device parameters stayed within datasheet limits at all times.

3.3.4. Electromigration for copper interconnect

With electronic devices seeing an increase in power density but with a reduction in size, copper pillars have emerged as one of the more popular new interconnect solutions due to their excellent electrical characteristics and heat dissipation [19]. Figure 3-21 illustrates how the copper pillars connect to a lead frame-based package and a chip.

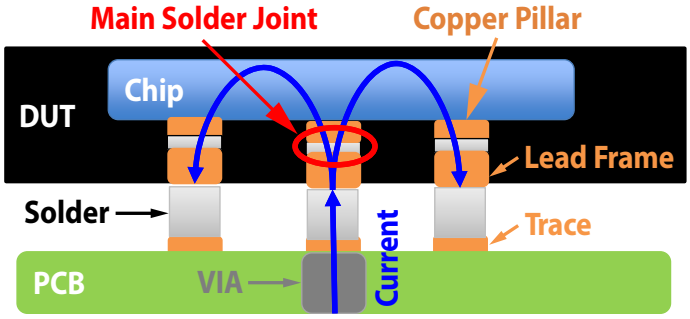


Figure 3-21 Copper pillar structure used in this work.

The pillar consists of two main structures including a solder cap and a cylindrical or elliptical copper. The solder cap serves as the sole interconnect between the device and the package, mainly composed of Tin (Sn) with varying trace amounts of Silver (Ag), Gold (Au), and Copper (Cu) [20-24]. The solder joint is a critical point of interest due to its lower current density rating and lower temperature melting point compared to copper.

Electromigration (EM) has been identified as a potential wear-out mechanism in the interconnects of power quad flat no-leads (PQFN) packages. EM is defined as the movement of atoms in metal structure, leading to void formation [25,26]. The primary cause of EM is the electron "wind" generated from the transfer of momentum between conducting electrons and metal ions in the crystal. When the momentum surpasses the diffusion threshold that is governed by an activation energy [25,26] metal atoms can move and create voids.

Two primary stressors responsible for EM void formation are high current density and high temperature [19-22]. Current density is expressed as the current divided by the area of contact between the two-metal interconnect. Temperature is typically expressed as the junction temperature of the interconnect in Kelvin unit.

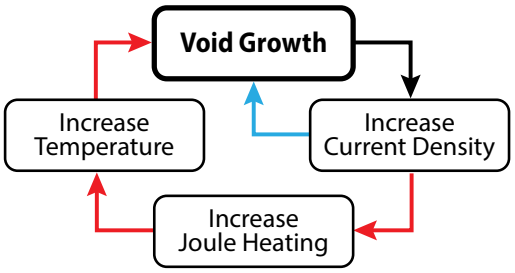


Figure 3-22: Void growth acceleration through positive feedback loop: current density generates voids, resulting in increased current density thus increasing temperature as a result of Joule heating at the point of contact thus voids growth is accelerated.

The Black's model is well accepted to predict lifetime under EM stress conditions, shown in Eq. 3-9 [25,26].

$$MTTF = Aj^{-n}e^{\frac{Q}{kT}} \quad \text{Eq. 3-9}$$

Where A is a constant, j is current density, n is an exponent, Q is the activation energy, k is the Boltzmann's constant at 8.62 x 10^{-5} eV/K, and T is the temperature in Kelvin unit.

Figure 3-22 shows two positive feedback loops. The first loop describes the void growth process accelerated by the current density [26], which is characterized by the current density power term in Equation 3-9. As the degradation of the interconnect begins through the formation of voids, the decrease of cross-sectional area leads to the further increase of current density, accelerating the void formation.

The second loop is dominated by the thermal activation process. Joule heating causes an increase in junction temperature, which further accelerates the movement of atoms resulting in more void formation. This process is described by the Arrhenius term, which is the last term in Equation 3-9.

Both processes could lead to an open circuit from void formation or electrical shorts from the melting metal interconnect. Due to EM being a slow mechanism that can take years to develop under use conditions, testing under accelerated stress conditions is necessary to generate EM related failures within a reasonable amount of time.

Experiments

The experiment is split into three parts including a device under test (DUT) card, a custom test chip, and a temperature chamber. The schematic of the DUT card for in-situ resistance monitoring is shown in Figure 3-23. The custom test chip was designed by following JEDEC standard, JEP154 [27].The test setup is placed in a temperature chamber with the DUT card placed in the center. Two thermocouples are deployed. One is mounted at the center of the oven to monitor the ambient temperature. The other one is placed directly on the backside of the DUT where the backside Si substrate is exposed. The test chip is covered with thermal putty and sandwiched between two copper heat sinks to maintain constant temperature of the test chip.

The temperature difference between the copper pillar interconnect and the backside of the device is calculated to be 0.64°C by using the $R_{th,JC}$ of 0.2°C/W and a total of 3.2 Watts of power dissipated at 125°C. The copper pillar interconnect of interest has an elliptical shape with an area of 5,271 μm^2 and is soldered onto a copper lead frame that is molded into a PQFN package outline.

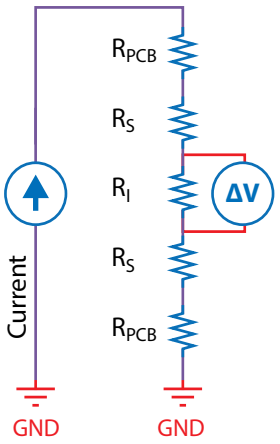


Figure 3-23: Schematic representation of the in-situ monitoring of the solder interconnect represented by R_I where the voltage drop is measured, R_S is the solder joint resistance of the package to the PCB and R_{PCB} represents the resistance of the copper in the PCB.

Results and Discussions

Test conditions of 27 kA/cm^2 at 125°C and 55 kA/cm^2 at 150°C were selected, based on previous research studies focusing on copper pillar interconnects [22-24,27]. A failure criterion of 10% resistance increase was adopted according to the recommendations in JEP154 [27].

Both test conditions yielded zero failures as shown in Figures 3-24 and 3-25. Figure 3-24 shows that after 480 hours of testing, no devices exceeded a 2% resistance increase. Similarly, Figure 3-25 shows that after 645 hours of testing under such extreme stress condition (55 kA/cm^2 at 150°C), no part exceeded the failure criterion of 10% resistance increase. Our results are consistent with various studies that focus on EM copper interconnects [20-24].

A current density power exponent of 2 has been frequently reported for copper pillar interconnects by various studies [20,23]. An activation energy of 1 eV is commonly accepted for SnAg solder cap through previous works [20-24]. By using the values of n=2 and Q=1 eV and assuming the time to failure of 645 hours at 0.1% failure rate,

the constant A from the Black's equation is calculated to be 2.39. By having the constant A, the lifetime at 0.1% failure rate at any given temperature and current density can be projected.

The continuous current ratings of EPC's PQFN devices [20,26] are based on a conservative EM current density limit of 10 kA/cm^2 . By plugging in a current density of 10 kA/cm^2 and a junction temperature of 125°C, greater than 11 years of lifetime at 0.1% failure rate is projected. The test is ongoing. Hence, a more accurate lifetime will be updated when failures are found.

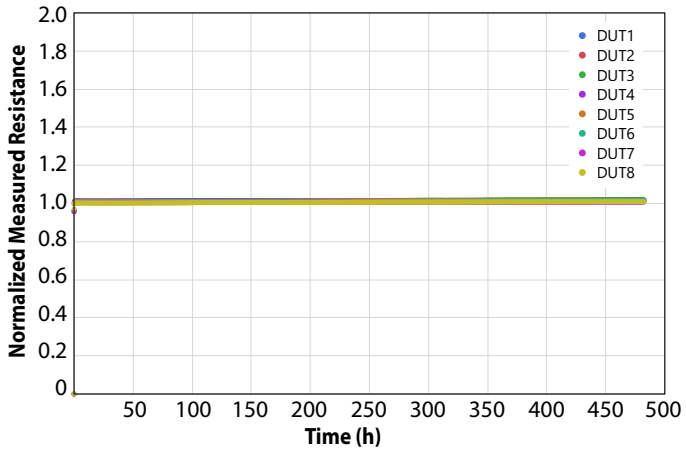


Figure 3-24: Normalized measured resistance of copper interconnect for 24kA/cm^2 at 125°C of 8 DUTs

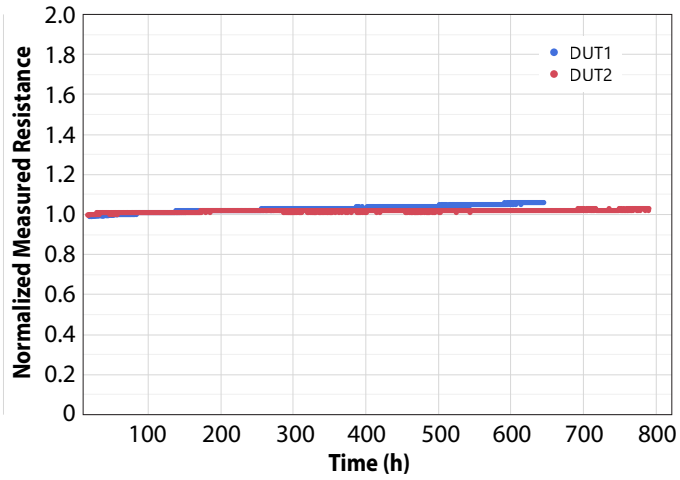


Figure 3-25: Normalized measured resistance of copper interconnect for 55kA/cm^2 at 150°C of 2 DUTs.

3.4. Thermo-Mechanical Wear-Out

3.4.1. Introduction to Thermo-Mechanical Wear-Out Mechanisms

Solder joint cracking, which occurs due to a mismatch in the coefficient of thermal expansion (CTE) between materials, has emerged as a common concern in applications that demand frequent and large temperature swings. A general temperature cycling (TC) lifetime model is developed in this section based on testing parts to failure. The lifetime model encompasses device dimensions, bump shape, stand-off height, and various PCB properties including modulus, Poisson's ratio, and PCB thickness. When the expected lifetime of chip scale packaged (CSP) devices is less than the customers' specifications, underfill with the right materials properties is recommended to improve TC lifetime. For packaged QFN parts, which intrinsically have relative low standoff height, it is critical to minimize the die tilt and to have consistent sidewall solder fillets connecting to the wettable flanks. Hence, a stencil design rule for QFN parts is provided to guide assembly.

3.4.2. Impact of Die Size and Bump Shape on Temperature Cycling (TC) Reliability

TC lifetime with respect to the die size is typically modeled by the classic Coffin-Manson relation, where the devices under test are usually symmetrical in both x and y directions [29]. In addition, most of the solder joints presented in those studies are ball grid array (BGA), where all the bumps have identical shape. Thus, distance-to-neutral point-based TC lifetime models are frequently adopted and have proven to be effective [30]. However, there is a lack of TC lifetime models that account for both asymmetrical die size and varying solder bump shapes with land grid array (LGA) solder bumps [31].

In this section, a suite of wafer level chip scale package (WLCSP) GaN devices with varying die size and bump shapes are studied under a consistent assembly and TC testing condition. TC lifetime model that includes all die sizes and bump shapes was developed and an excellent fit was achieved.

Solder Joint Cracking

In previous reliability reports [1,5], the main wear-out mechanism mode under temperature cycling (TC) stress is identified as solder joint cracking [1]. Coefficient of thermal expansion (CTE) mismatch between the materials namely the device, solder and PCB is attributed as the fundamental cause of this wear-out mechanism. The CTE values of a typical FR4 PCB [32], a wafer level chip scale package (WLCSP) device [33], and SAC305 solder [34] are given in Table 3-4. Figure 3-26 illustrates the resulting stress caused by CTE mismatch during temperature cycling testing.

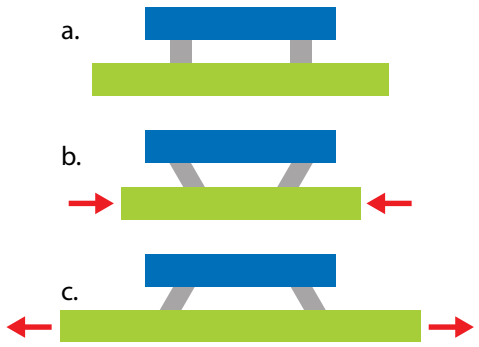


Figure 3-26: Illustration of stress on solder joints during temperature cycling

Figure 3-26(a) shows the solder joint between the device and PCB in a neutral thermal stress position. As the temperature is lowered as in Figure 3-26(b), the PCB with the higher CTE value contracts more than the GaN device, creating strain on the solder joints. Similarly, when the temperature increases in Figure 3-26(c), the PCB undergoes more expansion than the device, again creating strain on the solder joints.

Material	CTE (ppm/ °C)
Device	4
Solder	23
PCB (FR4)	18

Table 3-4: Common material coefficients of thermal expansion

Experiment

A suite of WLCSP GaN transistors with various dimensions are evaluated for temperature cycling performance, including EPC2206, EPC2071, EPC2069, EPC2218 and EPC2204 shown in Fig. 3-27.

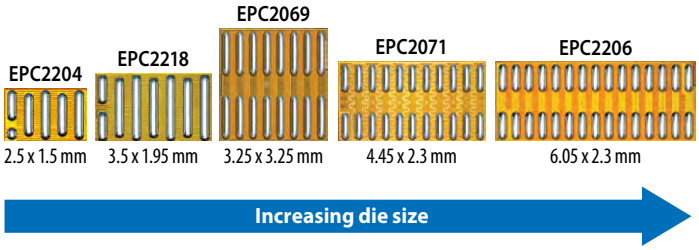


Figure 3-27: Devices tested in this study: EPC2204, EPC2218, EPC2069, EPC2071, and EPC2206

The temperature cycling experiment was constructed to ensure that the only variables are the device dimensions and bump shape. These devices were mounted on identical test PCB boards using identical solder (SAC305). The PCB boards consist of 2-layer Cu, 1.6-mm thick, FR4 board. The standoff height (i.e. the solder height after assembly) of ~130 µm was maintained during the assembly process. This was verified by performing physical cross-section of the assembled boards. The temperature cycle range was from -40°C to 125°C, with a ramp rate of 15°C/min and soak time of 10 minutes at the end points following industry standard JESD22-A104F [35].

A group of 88 devices were tested for each WLCSP device. After every temperature cycling interval, an electrical screening was performed, where an increase in $R_{DS(on)}$ exceeding datasheet limits was used to determine failures.

A test-to-fail approach was adopted, where the devices are tested until a 50% failure rate is achieved. The failure distribution was analyzed using a two-parameter Weibull distribution for each device using Maximum Likelihood Estimation (MLE) [36]. The resulting Weibull fits are indicated by solid lines in the graph of Fig. 3-28, and the Weibull characteristics are in Table 3-5. The gate solder joint cracking was found to be the single wear-out mode throughout all devices analyzed by physical cross-sectioning and SEM inspection, establishing that wear-out of the smallest solder bump is the limiting factor for temperature cycling lifetime.

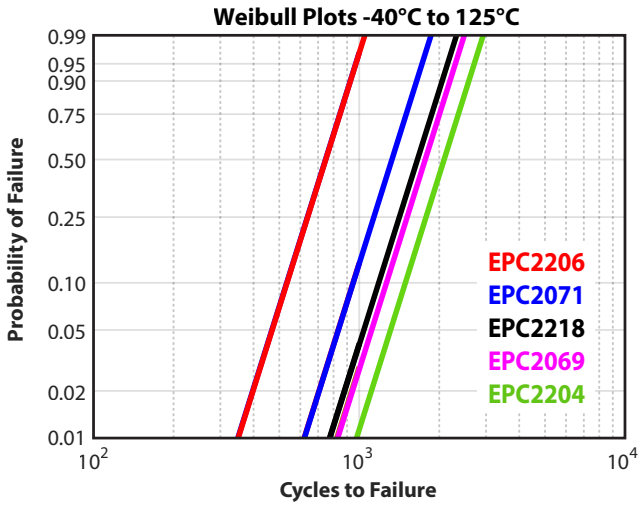


Figure 3-28: Weibull fits to experimental TC data.

Device	Weibull Shape Parameter	Characteristic Weibull Life (cycles)	MTTF (cycles)
EPC2206	5.6	797	737
EPC2071	5.6	1416	1309
EPC2218	5.6	1764	1630
EPC2069	5.6	1880	1737
EPC2204	5.6	2389	2208

Table 3-5: Weibull statistics for 5 tested devices

Effect of Die Shape on Temperature Cycling Lifetime

The Mean-Time-To-Fail (MTTF) data from the Weibull distribution, measured in number of cycles, were compared to die area to check for die size correlation with TC lifetime. The data is fit to

$$MTTF = A(Die\ Area)^{-n} \quad \text{Eq. 3-10}$$

where A is a constant, Die Area is the area of die by multiplying the length with the width and n is the exponent. The resultant fit is judged by goodness-of-fit (R^2). By fitting MTTF from Table

3-5 with Eq. 3-10 yielded an R^2 value of 0.67, indicating a poor fit. It suggests that that die area alone is unable to provide a good correlation with TC lifetime by following the commonly accepted lifetime models in literatures [37-39].

The concept of Maximum Distance from Neutral Point (DNP^{max}) is introduced as shown in Fig. 3-29. During TC stress, the center point of the device experiences the least stress compared to extremities of the device. This center point is defined as the neutral point, the distance from the neutral point to the farthest extremity of solder bump is defined as DNP^{max}.

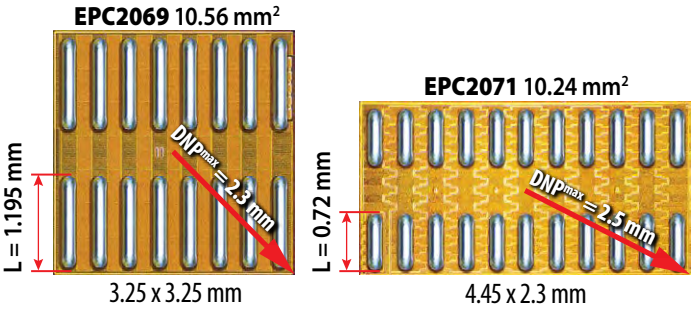


Figure 3-29: Example of gate length and DNP^{max} for EPC2069 and EPC2071

By combining Norris-Landzberg modified Coffin-Manson TC lifetime model [40] and the concept of DNP, Eq. 3-11 is developed as reported by multiple researchers [39].

$$MTTF = A(DNP^{max})^{-n} \quad \text{Eq. 3-11}$$

The best fit to Equation 3-11 yielded a R^2 value of 0.79, slightly improved compared with simply using the device area. However, it is still not considered a very good fit.

Failure analysis established the gate solder joint cracking at the device corner as the limiting factor for TC performance. A longer gate bump likely indicates a longer time to failure under TC stress and vice versa. Figures 3-27 and 3-29 show that different device sizes also have varying length of the gate solder bump. Therefore, the corner gate bump shape should also be considered along with the DNP^{max} for a more accurate TC lifetime model development. Because the gate bump width is similar for all devices studied, the bump length, denoted as L, is the primary parameter that is included in the following discussions. Thus, the length of solder bump L is factored into DNP^{max}, and effective DNP^{max} ,DNP^{eff} is defined in Equation 3-12.

$$DNP^{eff} = DNP^{max} + a \cdot L \quad \text{Eq. 3-12}$$

The resulting fit is shown in Figure 3-30 and results in an R^2 value of 0.99 using gate length factor a = -0.65, and power exponent n = 1.4.

The fitted power exponent of 1.4 shown in Figure 3-30 is consistent with other literature results [41-42], where exponents between 1 and 2 are frequently reported in SAC305 solder joint cracking failures under TC stress with similar test conditions.

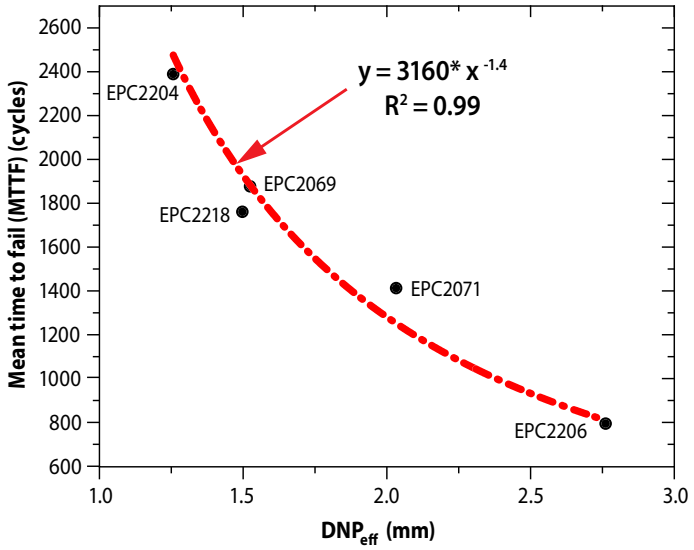


Figure 3-30: Comparing MTTF with effective DNP

In summary, a TC lifetime model is proposed considering the device size and corner gate bump shape,

$$MTTF = A(DNP^{max} - 0.65 \cdot L)^{-n} \quad \text{Eq. 3-13}$$

This study establishes a temperature cycling lifetime model based on solder joint cracking caused by CTE mismatch from materials which takes into consideration the varying dimensions of both die and solder joints.

3.4.3 Effect of PCB Properties on Temperature Cycling Lifetime

High-density power modules frequently utilize high-layer count, thick printed circuit boards (PCB). Such implementation raises concerns about solder joint reliability under temperature cycling (TC) due to the increased stiffness of these complex PCBs. In this section solder joint reliability of quad-flat no-leads (QFN) GaN transistors on PCBs with two different copper layer thickness was evaluated. A 10% lifetime acceleration was found when going from a PCB with 1 Oz Cu per layer to another PCB that has 2 Oz Cu per layer. A first principles lifetime model was adapted to study the lifetime difference, and an excellent agreement was found between the experiment and the modeled results. The modeling revealed that the TC lifetime associated with bending stiffness dominates, and accounts for 83% of the overall lifetime difference.

Temperature Cycling Testing and Failure Analysis

Two types of PCBs are evaluated for temperature cycling under the test conditions of -40°C to 125°C with 10 minutes dwell time at hot and cold temperature extremes. Both 2-layer PCBs use 2 layers

of copper, but the difference is that one PCB uses 1 Oz of Cu per layer. The other PCB uses 2 Oz of Cu per layer. The device under test (DUT) is EPC2302, a 100 V rated GaN QFN transistor. 104 QFN devices from each group were tested.

Table 3-6 shows the wear-out rate at every interim read point. Data sheet limits of EPC2302 are used as the failure criteria, where $R_{DS(on)}$ exceeding the datasheet maximum limit is the primary wear-out mode. A significant wear-out rate difference is observed starting from 1300 cycles. At 2000 cycles, a wear-out rate discrepancy of more than 40% is seen.

PCB Type	0 cycle	400 cycles	850 cycles	1300 cycles	1600 cycles	1800 cycles	2000 cycles
1 oz Cu	0.0%	0.0%	0.0%	1.0%	14.0%	26.0%	44.3%
2 oz Cu	0.0%	0.0%	0.0%	6.9%	21.8%	41.6%	62.9%

Table 3-6: Wear-out rate at each interim read point in TC.

Figure 3-31 shows the Weibull distributions of the two testing legs, where the two-layer PCB with 1 Oz Cu layer outperformed the other group with 2 Oz Cu per layer by approximately 10% in mean-time-to-fail (MTTF).

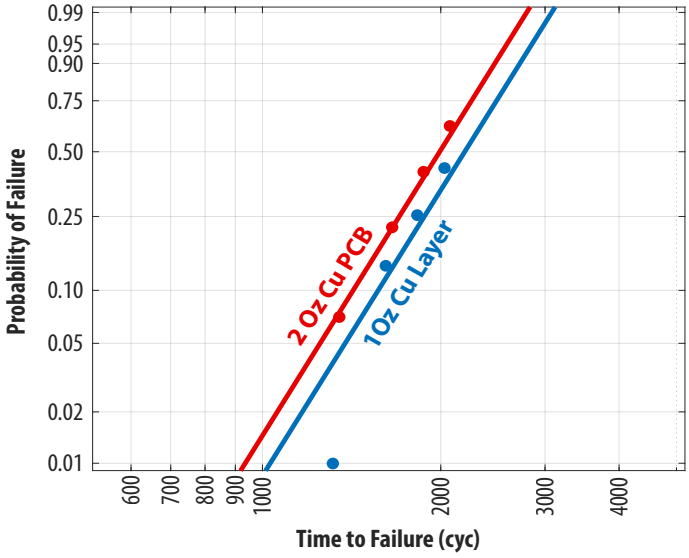


Figure 3-31. Weibull distribution of two testing legs. Leg 1 uses 2 layers of Cu with 2 Oz of Cu per layer. Leg 2 still uses 2 layers of Cu but with 1 Oz of Cu per layer.

The detailed stack-up of two types of PCBs studied are compared in Table 3-7. It is noted that the 2 Oz Cu PCB is approximately 2% thicker than the 1 Oz Cu PCB. The prevailing trends that have been reported in literature show that thicker boards generally lead to worse TC lifetime caused by a solder joint wear-out failure mode [37-39]. However, a 2% PCB thickness increase does not sufficiently explain the 10% lifetime reduction. There must be some other hidden parameter(s) that dominate TC testing results observed in the study.

1 Oz Cu PCB Stack-up		2 Oz Cu PCB Stack-up	
Layer	Thickness	Layer	Thickness
Top side solder mask	0.7 mils	Top side solder mask	0.7 mils
Top Cu layer	1.4 mils	Top Cu layer	2.8 mils
FR4	57.6 mils	FR4	56.2 mils
Bottom Cu layer	1.4 mils	Bottom Cu layer	2.8 mils
Bottom side solder mask	0.7 mils	Bottom side solder mask	0.7 mils
Total	61.8 mils	Total	63.2 mils
	1.570 mm		1.605 mm

Table 3-7: Details of the PCB stack-up of 1 Oz Cu PCB vs. 2 Oz Cu PCB

At each TC testing interval, parts were randomly selected for failure analysis. The gate corner solder joint cracking is found to be the consistent underlying wear-out root cause. Figure 3-32 shows the physical cross-section and followed with SEM inspection and Figure 3-33 shows the 3D X-ray cross sectional results of two different devices post TC testing. Both figures revealed that the crack likely initiated from the sharp QFN device corner. Following crack initiation, it likely propagated vertically along the sidewall wettable flanks as well as laterally along the exposed leads of QFN devices.

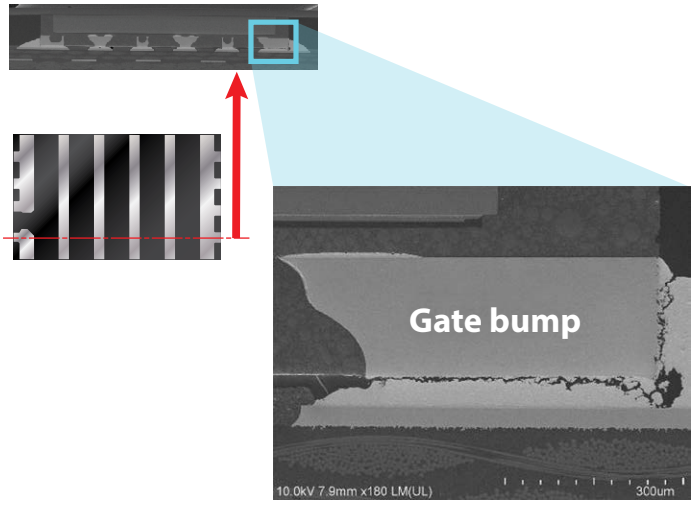
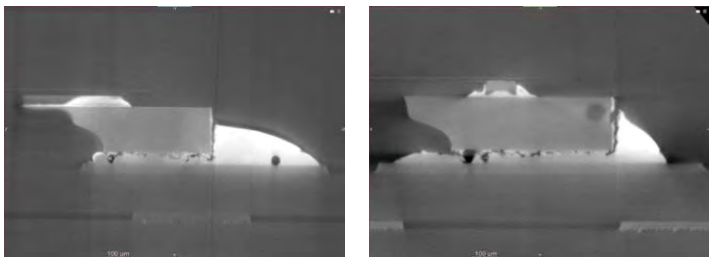


Figure 3-32: SEM images of a TC failure, where the gate solder joint at the QFN device corner is responsible for the wear-out.



(a) (b)

Figure 3-33: 3D X-ray cross-section with a focus on the gate corner solder joint, revealing the underlying wear-out mechanism.

COMSOL Finite Element Analysis (FEA) Simulation

COMSOL Multiphysics® software [45] was used to perform the modeling. Figure 3-35 shows the 3D geometry buildup of EPC2302 QFN device mounting on a PCB.

Figure 3-36(a) shows the 3D design of the sidewall fillets that closely resemble the actual finished assembly, as shown in optical image from Figure 3-36(b). Figure 3-36(c) highlights the fine meshes that were applied to the gate corner solder joint to closely estimate the thermo-mechanical stress caused by TC.

Figure 3-37 shows the simulated von Mises stress [46] distribution in a cross-sectional view of the gate corner solder joint by comparing two different PCB implementations. The high-stress point identified in the COMSOL simulation coincided with the gate corner crack that was found in the failure analysis (Figures 3-32 and 3-33). Such great consistency validates the accuracy of our FEA simulations, suggesting the gate corner concentrates stress during repetitive thermo-mechanical testing and leads to crack initiation and propagation. A similar finding on QFN device assembly was also reported by Rahangdale et al. [44].

The stress difference between the two assemblies (1 Oz Cu PCB vs. 2 Oz Cu PCB) is quantified by COMSOL simulation. The average von Mises stress along the gate corner edge in 1 Oz Cu PCB, where the highest stress is seen, is estimated to be 201.7 MPa. By comparing with the 2 Oz Cu PCB, the average von Mises is calculated to be 233.3 MPa, which is 15.7% higher than the stress observed in 1 Oz PCB assembly. A 15.7% stress increase agrees with the 10% lifetime reduction shown in Figure 3-31.

The overall lifetime, N_{Total}, consists of three parts of life which associate three different mechanical coupling mechanisms [37]. The first part, N_1, is the lifetime that is characterized by the in-plane tensile shear force, acting on the device. Figure 3-34 illustrates the evolution of the dimensional changes of a device and a PCB when the ambient temperature increases from a low temperature, where the stress on the solder joints is neutral, to the hot temperature extreme where the device expands significantly less than the PCB due to the CTE mismatch. As a result, the solder joints are stretched laterally as shown in Figure 3-34.

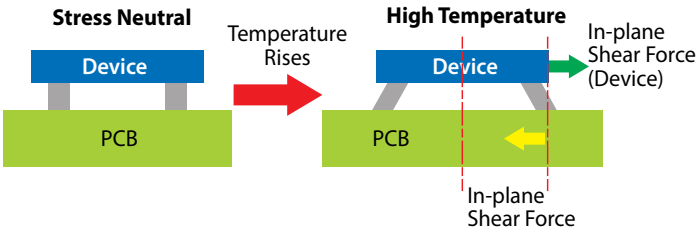


Figure 3-34: Illustration of the in-plane tensile shear forces acting on the device and PCB.

N_1 represents the in-plane tensile stiffness of the mounted device as shown by the green arrow in Figure 3-34. Equation 3-14 specifies the lifetime caused by such in-plane stencil shear force.

$$N_1 = \frac{F}{\Delta\alpha^2} \times \frac{1-\gamma_{QFN}}{E_{QFN}h_{QFN}} = \frac{F}{\Delta\alpha^2} \times C_1 \qquad \text{Eq. 3-14}$$

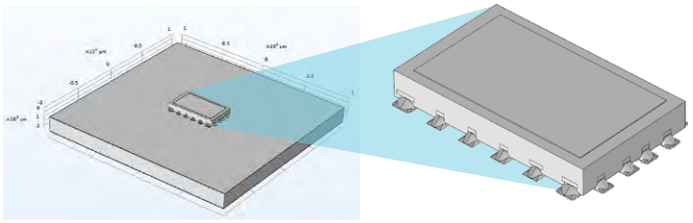


Figure 3-35: 3D buildup of an EPC2302 QFN device that is surface mounted on a PCB.

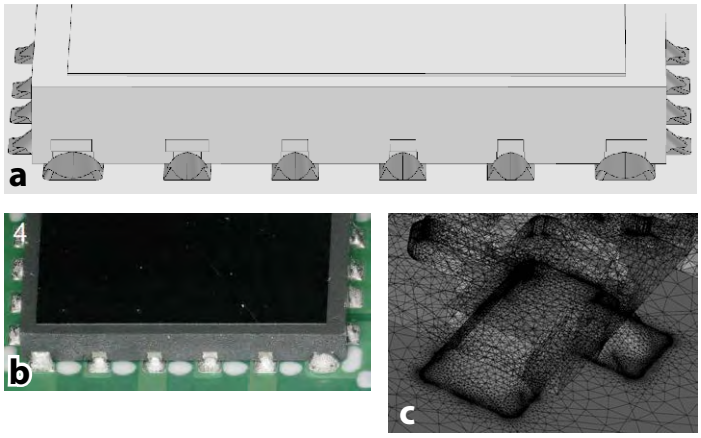


Figure 3-36: (a) shows the sidewall fillets in the COMSOL simulation. (b) shows the side view optical image of the sidewall fillets post assembly. (c) shows the fine meshes applied to the gate corner solder joint.

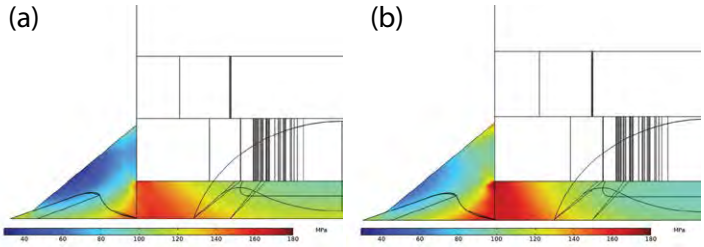


Figure 3-37: Cross-sections of the COMSOL simulation results at the gate corner solder joint. (a) 1 Oz Cu per layer PCB with an average von Mises stress of 201.7 MPa along the high stress corner; (b) 2 Oz Cu per layer PCB with an average von Mises stress of 233.3 MPa along the high stress corner.

where F is a constant for a specific device-PCB system and under a given TC stress condition, Δα is the CTE mismatch between the device and PCB, γ_{QFN} is the Poisson's ratio of the device, E_{QFN} is its Young's modulus, and h_{QFN} is the height of the device. C_1 is denoted as the axial compliance of the device, $C_1 = \frac{1-\gamma_{QFN}}{E_{QFN}h_{QFN}}$.

The second term, N_2, is controlled by the in-plane tensile shear force that acts on the PCB as highlighted by the yellow arrow in Figure 3-34. Equation 3-15 characterizes the corresponding lifetime that is related to such tensile stiffness of the PCB.

$$N_2 = \frac{F}{\Delta\alpha^2} \times \frac{1-\gamma_{PCB}^2}{2E_{PCB}h_{PCB}} = \frac{F}{\Delta\alpha^2} \times C_2 \qquad \text{Eq. 3-15}$$

where F and Δα are the same as in Equation 3-14, γ_PCB is the Poisson's ratio of the PCB, E_{PCB} is its Young's modulus, and h_{PCB} is the PCB thickness. C_2 is defined as the axial compliance of the PCB, $C_2 = \frac{1-\gamma_{PCB}^2}{2E_{PCB}h_{PCB}}$.

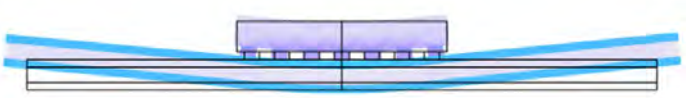


Figure 3-38: COMSOL FEA simulation results illustrate the flexural bending between the device and PCB.

Lastly, N_3 represents the bending moments of the bimetallic strip of the device and PCB. Figure 3-38 shows the FEA simulation result of such bending motion. This part of lifetime, N_3, is dominated by the flexural modulus of the QFN device and the PCB.

$$N_3 = \frac{F}{\Delta\alpha^2} \times \frac{H^2}{\frac{E_{QFN}^f h_{QFN}^3}{12(1-\gamma_{QFN})} + \frac{E_{PCB}^f h_{PCB}^3}{6(1-\gamma_{PCB}^2)}} = \frac{F}{\Delta\alpha^2} \times C_3 \qquad \text{Eq. 3-16}$$

Where E^f_{QFN} and E^f_{PCB} are the flexural Young's modulus of the QFN device, respectively. C_3 is the bending compliance of the bimetallic strip assembly of the device and PCB,

$$C3 = \frac{H^2}{\frac{E_{QFN}^f h_{QFN}^3}{12(1-\gamma_{QFN})} + \frac{E_{PCB}^f h_{PCB}^3}{6(1-\gamma_{PCB}^2)}}$$

and H is further defined by Equation 3-17.

$$H = \frac{h_{QFN}}{2} + h_{standoff} + \frac{h_{PCB}}{2} \qquad \text{Eq. 3-17}$$

where $h_{Standoff}$ is the standoff height of the solder joint, post-assembly. Therefore, the total lifetime N_{Total} is determined by the sum of all three parts, as shown in Equation 3-18.

$$N_{Total} = N_1 + N_2 + N_3 = \frac{F}{\Delta\alpha^2} \times (C_1 + C_2 + C_3) \qquad \text{Eq. 3-18}$$

Table 3-8 summarizes all the key parameters that are used for the TC lifetime modeling of the QFN device and a 2-layer Cu PCB system.

Based on the parameters listed in Table 3-8, the common constant F in Equations 3-14 through 3-16 can be estimated. Therefore, every part of the lifetime (N_1, N_2, N_3) and the overall lifetime, N_{Total}, can be modeled.

Figure 3-39 plots the modeled overall TC lifetime of 1 Oz Cu PCB and 2 Oz Cu PCB as a function of PCB thickness. At 1.6 mm PCB thickness, a lifetime difference of 187 cycles was identified as highlighted by the green arrow. The modeled result agrees well with the measured results of 183 cycles in life difference. Table 3-9 summarizes the measured MTTF and the modeled result, where an excellent agreement is found.

	1Oz Cu PCB	2Oz Cu PCB	Unit
E_{QFN}	112	112	GPa
h_{QFN}	0.65	0.65	mm
v_{QFN}	0.22	0.22	
E_{PCB}	26.4	30.7	GPa
h_{PCB}	1.57	1.6	mm
v_{PCB}	0.16	0.17	
$h_{standoff}$	0.05	0.05	mm
H	1.16	1.175	mm
C_1	0.011	0.011	
C_2	0.012	0.010	
C_3	0.065	0.056	
$C_1 + C_2 + C_3$	0.087	0.076	

Table 3-8: Key parameters that are used for the TC lifetime projection. The modulus and Poisson's ratio are estimated based on the respective weighted percentage of the composing materials.

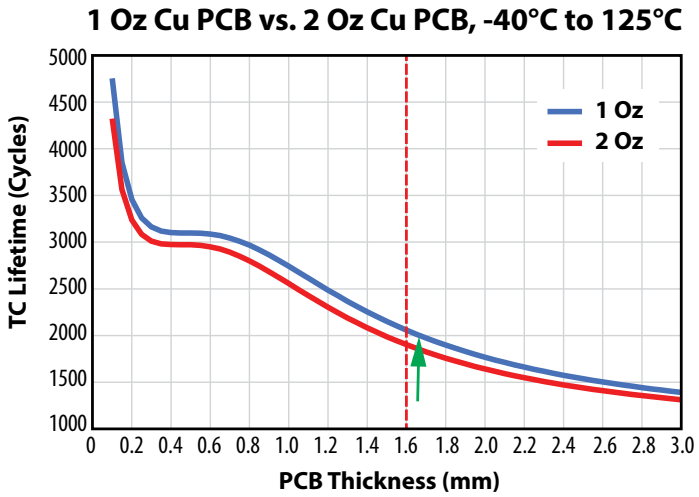


Figure 3-39. Modeled overall lifetime of two difference PCB stack-up as a function of PCB thickness. An approximately 10% lifetime difference is found at 1.6 mm thick.

Since a first principles modeling approach was adopted, each individual lifetime of in-plane tensile stresses and bending compliance are estimated and summarized in Table 3-9. The N_3 part of life, controlled by the bending flexural rigidity contributes to 83% of the overall lifetime decrease when using 2 Oz Cu PCB. The rest of the contribution (17%) comes from the axial shear stress acting on the PCB. Therefore, the 2% PCB thickness increase from 1 Oz Cu PCB to 2 Oz Cu PCB is not the dominant factor responsible for the 10% characteristic TC lifetime difference. The modulus difference shown in Table 3-8 predominates. Such trend is consistent with what de Vreis et al previously reported [43].

PCB Type	Measured MTTF (Cycles)	Modeled Life (Cycles)	Modeled N_1 (Cycles)	Modeled N_2 (Cycles)	Modeled N_3 (Cycles)
1 Oz Cu PCB (-40°C to 125°C)	2086	2085	394	411	1280
2 Oz Cu PCB (-40°C to 125°C)	1903	1898	394	380	1125
ΔLife (1 Oz - 2 Oz)	183	187	0	31	156
ΔLife/Modeled Life			0%	17%	83%

Table 3-9: Measure MTTF vs. Modeled Lifetimes of 1 Oz Cu PCB and 2 Oz Cu PCB

In this work, the modulus change caused by increasing Cu content in the PCB is the dominant contributing factor that reduces the overall solder joint lifetime under temperature cycling stress. The modeled results showed an excellent agreement with the measured characteristic lifetime based on the Weibull analysis. COMSOL FEA simulation results also validate such findings.

3.4.4. Criteria for Choosing a Suitable Underfill

The selection of underfill material should consider a few key properties of the material as well as the die and solder interconnections. Firstly, the glass transition temperature of the underfill material should be higher than the maximum operating temperature in application. Also, the CTE of the underfill needs to be as close as possible to that of the solder since both will need to expand/contract at the same rate to avoid additional tensile/compressive stress in the solder joints. Note that when operating above the glass transition temperature (Tg), the CTE increases drastically. Besides Tg, and CTE, the Young (or Storage) Modulus is also important. A very stiff underfill can help reduce the shear stress in the solder bump, but it increases the stress at the corner of the device, as it will be shown later in this section. Low viscosity (to improve underfill flow under the die) and high thermal conductivity are also desirable properties.

Manufacturer	Part number	CTE (ppm/C)			Storage modulus (DMA) at 25°C (N/mm^2)	Viscosity at 25°C	Poisson's ratio
		Tg (TMA) [C]	Below Tg	Above Tg			
HENKELS LOCTITE	ECCOBOND-UF 1173	160	26	103	6000	7.5 Pa*S	
NAMICS	U8437-2	137	32	100	8500	40 Pa*S	0.33
NAMCIS	XS8410-406	138	19	70	13000	30 Pa*S	

Table 3-10: Material properties of underfill materials that are tested and proven effective to improve TC reliability of CSP devices.

The main guidelines for choosing an underfill for use with GaN transistors are listed below:

- Underfill CTE should be in the range of 16 to 32 ppm/°C, centered around the CTE of the solder joint (24 ppm/°C). Lower values within this range are preferred because they provide better matching to the die and PCB.
- Glass transition temperature (Tg) should be comfortably above the maximum operating temperature. When operated above Tg, the underfill loses its stiffness and ceases to protect the solder joint.
- Young's (or Storage) modulus in the range of 6–13 GPa. If the modulus is too low, the underfill is compliant and does not relieve stress from the solder joints. If it is too high, the high stresses begin to concentrate at the die edges.

Finite Element Analysis

To better understand the key factors influencing thermo-mechanical reliability when using underfills, finite element simulations of EPC2206 under temperature cycling stress were conducted. Figure 3-40 shows the simulation deck used for this analysis. The die is placed on a 1.6 mm FR4 PCB, and the temperature change is ΔT = +100°C above the neutral (stress free) state. Two key underfill parameters were varied: Young's modulus and CTE. As shown in the figure, stress is analyzed along the cut line shown, providing visibility into the stress within the solder bars, die, and underfill.

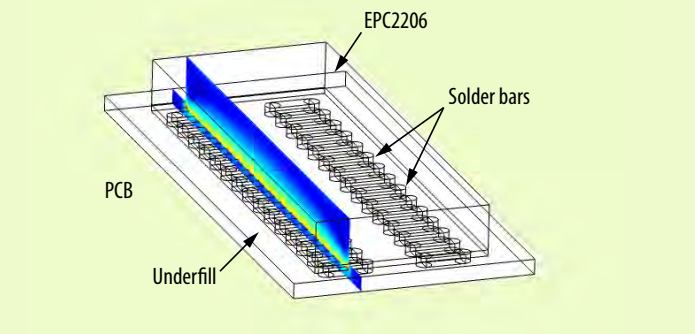


Figure 3-40: Simulation deck for finite element analysis of stresses inside EPC2206 under temp cycling stress. Die with underfill sitting on 1.6 mm FR4 PCB. Stress is analyzed along cut line shown.

Figure 3-41 shows the von Mises [46] peak shear stress in the edge-most solder bar along the cutline. For clarity, only stress in the solder bar is shown. In addition, mechanical deformations are exaggerated by 20 times in order to illustrate the shear displacement in the joint. Four distinct underfill conditions are simulated by changing the Young's modulus (E) or the CTE of the underfill. As can be seen, the solder bar in the no underfill case has by far the most extreme shear stress and deformation. The addition of underfill significantly alleviates stress from the joint. Higher Young's modulus reduces this stress further. For underfills with poor CTE matching to the solder joint, stress can also build up in the joint.

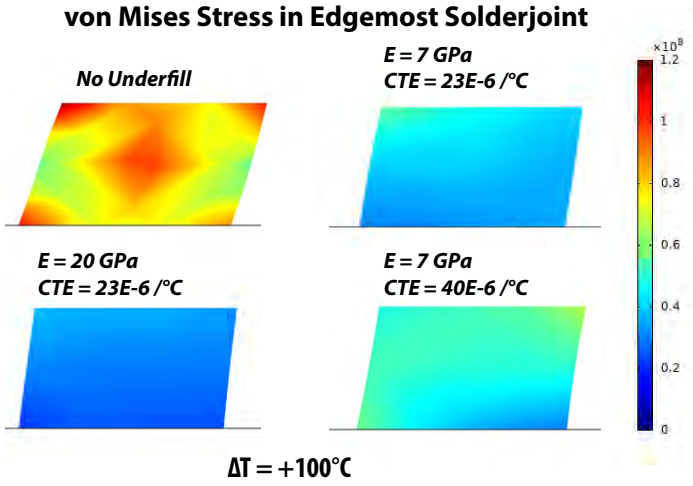


Figure 3-41: von Mises (peak shear stress) in the edge-most solder bar under a temperature cycle change of ΔT = +100°C. Four different underfill conditions are simulated, with changing Youngs modulus of the underfill, and different CTE as well. Note that mechanical deformation has been exaggerated by 20x in all cases.

Figure 3-42 shows the same four conditions, but this time the von Mises stress is shown in both the die and underfill. The high Young's modulus cases show low stress in the solder joint, but high stress inside the die and underfill near the die edge. These high stresses can lead to cracking and ultimate failure inside the device.

FEA analysis shows that there is an optimal Young's modulus in the range of ~6 to 13 GPa, providing a good compromise between protecting the solder joint and protecting the die edge. Regarding CTE, the analysis shows that high underfill CTE (> 32 ppm/°C) should be avoided.

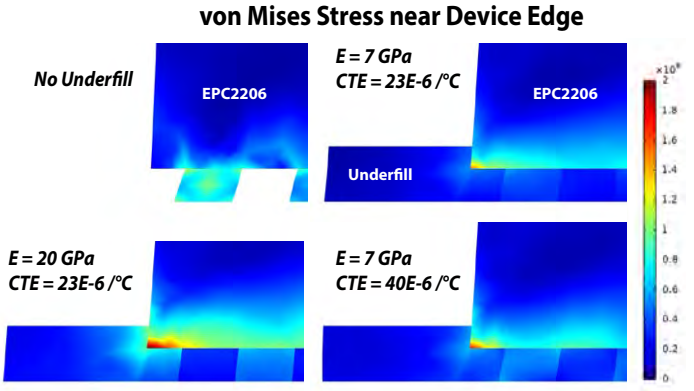


Figure 3-42: von Mises (peak shear stress) in the edge-most solder bar under a temperature cycle change of ΔT = +100°C. Four different underfill conditions are simulated, with changing Youngs modulus (E) of the underfill and different CTE as well. Note that deformation has been exaggerated by the same scale in each picture.

Experiment

The effect of underfill on temperature-cycling reliability was studied using EPC2218A [47], the automotive grade of the EPC2218, is a 100-V rated FET sold in chip-scale format.

Three different combinations of temperature cycling stress conditions, with and without underfill material were studied. Two temperature cycling ranges were tested: temperature cycle 1 (TC1): –40°C to 125°C and temperature cycle 2 (TC2): –40°C to 105°C.

Over the temperature range of TC1, two cases were compared: one with and one without underfill material. The underfill material selected was from Henkels Loctite (part number: Eccobond-UF 1173) which showed good performance in previous studies [5].

For all cases, the parts were mounted on DUT cards consisting of a two-layer, 1.6-mm thick, FR4 board using SAC305 solder paste, and water-soluble flux. All underfilled devices were subjected to a plasma clean process prior to the underfill application. Industry standard (JESD22-A104F [48]) as well as other customers' specifications were followed for this study.

A group of 88 EPC2218A devices were tested for each test leg, and all three legs used similar ramp rate and dwell time at the two temperature extremes. After every temperature cycling interval, electrical screening was performed. Exceeding datasheet limits was used as the criterion for failure. Physical cross-sectioning and SEM inspection were followed to further examine the electrical test failures. Solder joint cracking was found to be the single failure mode throughout all failures analyzed. The experimental results from the test-to-fail approach are summarized in Weibull plots in Fig. 3-43.

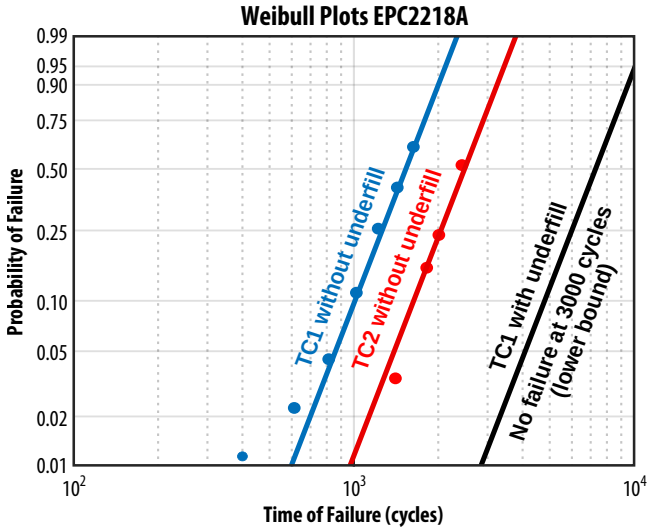


Fig. 3-43. Weibull plots of temperature cycling results for EPC2218A

The TC1 (–40°C to 125°C) tests without underfill material reached more than 50% cumulative failures at 1600 cycles, where physical failure analysis found that solder joint cracking was the single failure mode for all failures at various read points. The TC2 (–40°C to 105°C) tests without underfill achieved 50% failure rate after 2400 cycles. The data in Fig. 3-43 shows that a larger temperature range accelerates the time of failure in TC stress. After 3000 cycles of TC1 (–40°C to 125°C) with Henkel underfill, no outlier devices were found in the absolute $R_{DS(on)}$ value, nor in $R_{DS(on)}$ shift post electrical testing. All parameters examined showed very tight distributions throughout all temperature cycling intervals. Physical cross-sectioning was con-

ducted randomly on the 3000-cycle passing devices, where no solder joint cracking was observed. This shows that applying proper underfill material can significantly improve the TC capability of the chip-scale package devices. Therefore, the Weibull fit line for the TC1 with the underfill leg is merely the lower bound confidence level based on the current test results.

To understand the main failure mechanisms involved in board-level temperature cycling, the Norris-Landzberg lifetime model was adopted shown in Equation 3-19 [49].

$$N = A \cdot f^{-\alpha} \cdot \Delta T^{-\beta} \cdot exp\left(\frac{E_a}{kT_{Max}}\right) \quad \text{Eq. 3-19}$$

where N is the number of cycles to fail, f is the cycling frequency and α is the cycling frequency exponent. This frequency term f is to describe the frequency of usage.

In this study, the cycling frequency is determined by counting the total number of cycles per day. The cycling frequency exponent α is -1/3 [50-53]. ΔT is the range of temperature change in one cycle and β is the temperature range exponent. The temperature range exponent β is typically around 2. Since SAC305 solder is used in this study, a value of 2.3 for β is used [50-53].

The last variable is an Arrhenius term that focuses on the creep failure mechanism at the maximum temperature, T_{Max} in each cycle, where E_a is the activation energy, k is the Boltzmann constant, and T_{Max} is the maximum temperature of the high-temperature dwell stage in Kelvin (K). The activation energy (E_a) at T_{Max} was calculated to be 0.18 eV.

TC Condition	T_{min} (°C)	T_{max} (°C)	Characteristic Weibull Life	MTTF (cycles)
TC1 without underfill	165	40	36	1505
TC2 without underfill	145	30	48	2430
TC1 with underfill	165	40	36	7230 (Lower bound confidence level)

Table 3-11. Temperature cycling profile and MTTF determined by Weibull plots

This study forms the basis for the temperature-cycling reliability analysis of solar and DC-DC converters presented in Sections 4.1.6 and 4.2.5, respectively.

3.5. Mechanical Stress Wear-Out

3.5.1. Introduction to Mechanical Stress Wear-out Mechanisms

The lifetime of a product, or its suitability in applications, may be limited by the mechanical stresses encountered. In this section, some of the most common mechanical stressors, die shear, backside pressure, and bending force are characterized. The CSP and QFN package are demonstrated to be robust under normal assembly or mounting conditions.

3.5.2. Die Shear Test of Chip-Scale Parts

The purpose of die shear test is to evaluate the integrity of the solder joints used to attach eGaN devices to PCBs. This determination is based on the in-plane force at which, when applied to a mounted device, the die shears from the PCB. All testing followed the military test standard, MIL-STD-883E, Method 2019 [54].

Figure 3-44 shows the test results of four selected GaN transistors. Ten parts were tested for each product. The smallest die tested is EPC2036/EPC2203, which only has four solder balls with a diameter of 200 µm and a die area of 0.81 mm^2. As expected, this product turned out to have the least shear strength, however, it exceeds the minimum force requirement specified by the MIL standard, as shown in Figure 3-44. The largest die tested was EPC2206, a land grid array (LGA) product with die area of 13.94 mm^2. EPC2206 exceeds the minimum force requirement more than a factor of ten. Within the size spectrum, two additional products were tested: EPC2212 (100 V LGA) and EPC2034C (200 V BGA). Both products surpassed the minimum force significantly.

In Figure 3-44, the results show that all WLCSP GaN products are mechanically robust against environmental shear stress under the most stringent conditions.

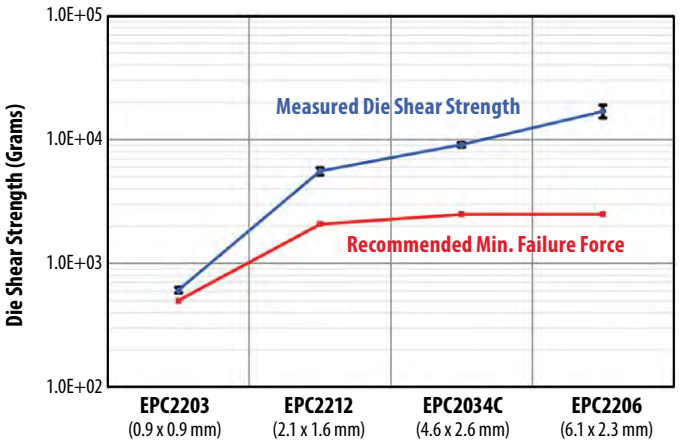


Figure 3-44. Various die sizes and solder configurations of GaN transistors were tested to failure while measuring the shear strength. The results are shown with black dots. The red dots show the minimum recommended die shear strength under MIL-STD-883E, Method 2019.

3.5.3. Backside Pressure Test of Chip-Scale Parts

Another critical aspect of the mechanical robustness of GaN devices is how well they handle backside pressure. This is an important consideration for applications that require backside heatsinking to the die. It is also important to determine the safe "pick-and-place" place force during assembly.

Backside pressure tests up to 400 psi were performed, where the pressure is calculated by the force applied divided by the die area. The pressure was applied directly to the backside of the die using a loading speed of 0.6 mm/min. Before and after the pressure test,

parametric testing was performed to determine pass or fail. Subsequently, the parts were exposed to humidity- bias testing (H3TRB) at 60 V_{DS}, 85°C, and 85% relative humidity for 300 hours. H3TRB is effective to determine if there were any latent failures caused by mechanical damage (internal cracking) from the pressure test.

EPC2212 (100 V, LGA) and EPC2034C (200 V, BGA) were tested, and both passed 400 psi. The 400 psi is calculated by normalizing the force applied on the backside of the device (Si substrate) to the die area. Results show that GaN transistors have enough margin to handle backside pressure that is normally used at a PCB assembly house. Though these parts survived 400 psi, backside pressure should be limited to 50 psi or less.

3.5.4. Bending Force Test of Chip-Scale Parts

The purpose of the bending force test is to determine the ability of a GaN transistor to withstand flexure of the PCB, which might occur during handling, assembly, or operation. Though this test standard was developed for passive surface mount components (AEC-Q200) [55], many customers have concerns about bending forces on GaN transistors for two main reasons:

1. Robustness of the WLCSP solder joints;
2. Piezoelectric effects within the transistor that may alter device parametric values and disrupt circuit operation.

To address these concerns, bending force testing on four EPC2206 devices following the AEC-Q200-005A test standard [61] were conducted. Devices are assembled near the center of an FR4 PCB (100 mm long x 40 mm wide x 1.6 mm thick). With ends rigidly clamped, a force is applied on the opposite side from the device, leading to an upward deflection of the PCB. After a 60 second dwell in this flexed state, all device electrical parameters are measured.

Table 3-12 shows normalized $R_{DS(on)}$ versus board deflection for all four devices under test. All devices passed the 2-mm test requirement. Two devices failed at 6-mm deflection, while the remaining two survived all the way to 8 mm. Postmortem analysis revealed that the failure mode was solder joint cracking, leading to an open gate connection. Up until failure, $R_{DS(on)}$ did not show any appreciable response to board flexure. The same result was observed in other electrical characteristics like V_{TH} and I_{DSS}.

	0 mm	2 mm	4 mm	6 mm	8 mm
DUT1	1.00	1.01	1.00	0.98	0.98
DUT2	1.00	1.02	1.01	*Failed*	-
DUT3	1.00	1.01	1.03	*Failed*	-
DUT4	1.00	0.99	0.99	1.03	1.04

Table 3-12:. Normalized $R_{DS(on)}$ versus board deflection for four devices during bending force test

Note: Values are normalized to the $R_{DS(on)}$ in the unflexed case. Two of four devices failed at 6 mm deflection, while the remaining two devices survived 8 mm. No significant stress response was seen in any device parameter.

3.5.5. Bending Test on PQFN Parts

PCB bending test was conducted to evaluate the solder joint robustness between the power quad-flat no-leads (PQFN) package devices and PCB under PCB bending and warpage stress conditions. These tests will address the customers' concerns in the module assembly, handling, and operations when potential mechanical impacts are present, such as PCB deformation in the motor drive applications and mechanical shock and PCB bending in automotive-related applications. The bending test uses a 3-point bending setup, following the Substrate Bending Test as described in IEC-60068-2-21. The devices are assembled at the center of an 8-layer PCB with the size of 180 mm long, 90 mm wide, and 1.6mm thick. The PCB is placed on two supporting fixtures with a 90mm gap. The device under test is placed facing down. The bending tool applies the force downwards at the back of the PCB to force the bending deflection. The test setup is shown in Figure 3-45.

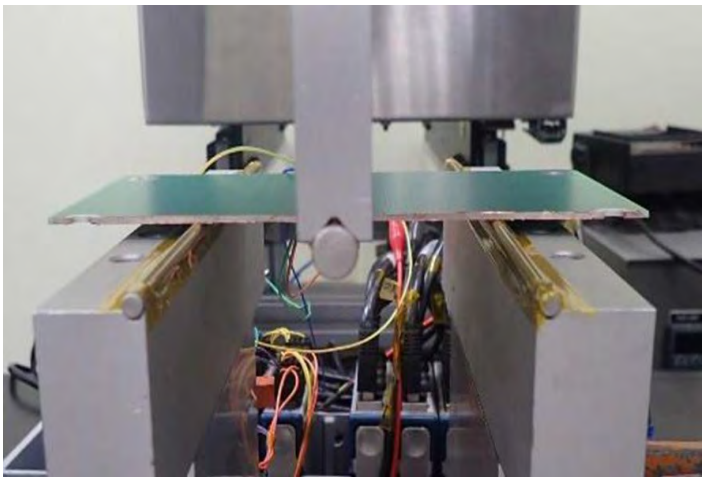


Table 3-45. Setup of the bending test

Test vehicle

Daisy-chain PQFN devices are used to enable reliable in-situ monitoring of the solder joint resistance during the test. The daisy-chain PQFN devices are developed and manufactured using the same PQFN component layout, constructions, and materials as the EPC2302. The only difference made is the back-end metal routing in the inside GaN-on-Si die. Combined with the specifically designed PCB, the daisy-chain connection through the solder joints between the PCB and the daisy-chain PQFN devices is achieved, as shown in the schematics in Figure 3-46.

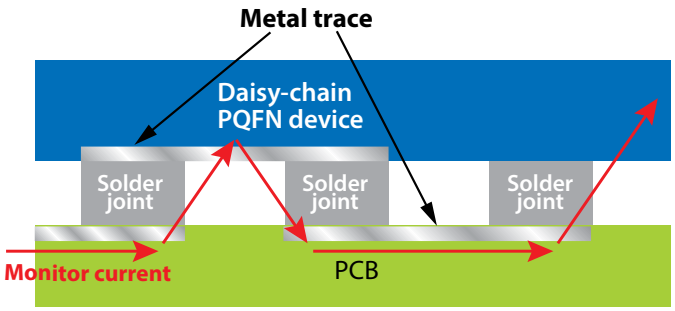


Figure 3-46: Schematics of the daisy-chain connection

Test conditions and results

The first test condition evaluates the solder joint robustness under constant load. 10 devices were stressed up to 2 mm bending deflection over 20s duration. The resistance of the daisy-chain devices was in-situ monitored during the bending test. Table 3-13 shows the resistance of each device before and after the test. For all the 10 devices, the resistance change is minimal, suggesting that no degradation in the solder joint is generated from this test.

Item	Sample No.	Pre-Test Resistance (Ω)	Post-Test Resistance (Ω)
Condition 1	1	0.21	0.22
	2	0.20	0.20
	3	0.20	0.21
	4	0.20	0.19
	5	0.22	0.22
	6	0.19	0.18
	7	0.19	0.18
	8	0.17	0.18
	9	0.20	0.19
	10	0.19	0.20

Table 3-13: Resistance before and after the first test to 2 mm deflection

To further verify the solder joint quality, three devices were randomly picked for solder joint cross-section inspection, as shown in Figure 3-47. The cross-sections are orthogonal to the bending direction. There are no observable solder joint cracks in the cross-sections, which agrees with the resistance records. Thus, these results show that the PQFN solder joints can handle constant load from PCB bending with a high level of reliability.

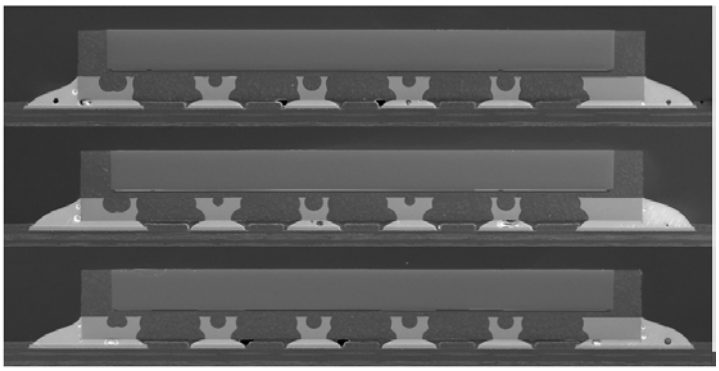


Figure 3-47: Cross-sectional images of solder joint robustness under constant load

Table 3-14 shows the resistance record before and after the bending test, and the max bending deflection. All the devices passed the bending deflection up to 10 mm, where insignificant amount of resistance change was observed. Two devices failed at approximately 11 mm of bending deflection. Failure analysis was conducted on the two failure devices and revealed that the failure mode is cracks in the GaN-on-Si die, as shown in Figure 3-48. Solder joint cross-sections were conducted on the failure die, which did not show observable solder joint cracks. Thus, the PQFN devices can survive PCB bending up to 10 mm, without observable degradations in the solder joints.

Item	Sample No.	Pre-Test Resistance (Ω)	Post-Test Resistance (Ω)	Max deflection (mm)
Condition 2	1	0.27	0.26	15.00
	2	0.26	1.78	11.36
	3	0.24	0.24	15.00
	4	0.23	0.23	15.00
	5	0.26	0.26	15.00
	6	0.23	0.22	15.00
	7	0.22	0.23	15.00
	8	0.21	0.22	15.00
	9	0.23	0.23	15.00
	10	0.23	0.86	10.82

Table 3-14: Resistance before and after the second test to 10 mm deflection, and the max bending deflection

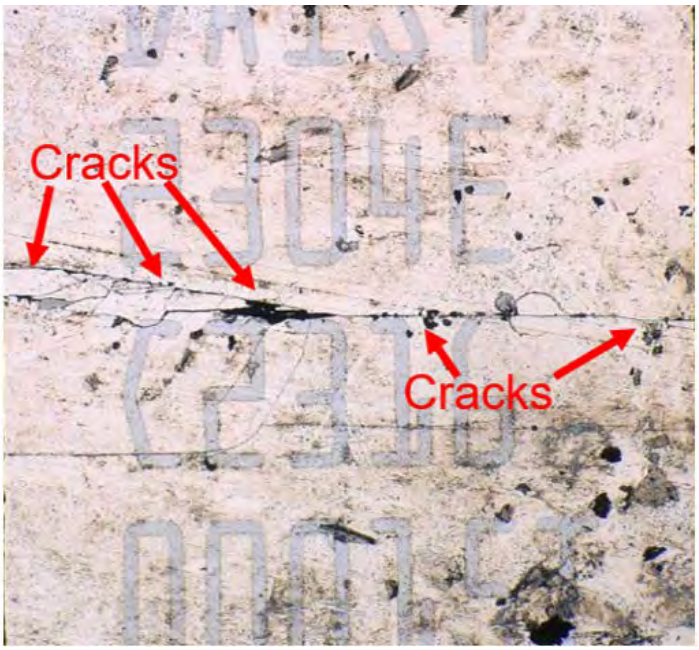


Figure 3-48: Cracks in the GaN-on-Si die

The failures of samples #2 and 10 occurred suddenly, without any observable degradation during tests at lower deflection, as shown in Figure 3-49.

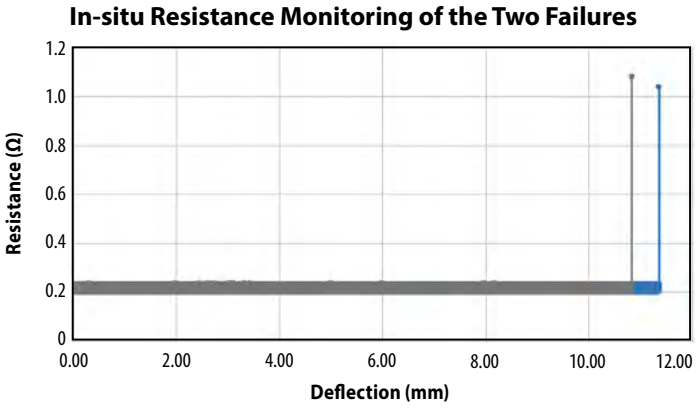


Figure 3-49: In-situ resistance monitoring results of the two failures

SECTION 4: MISSION-SPECIFIC RELIABILITY PREDICTIONS

Section 2 introduced a theoretical framework for analyzing device lifetimes in applications that include stress conditions of different intensities and durations. In this section that framework is applied to three example applications: solar, DC-DC, and lidar.

4.1. Solar Application Specific Reliability

4.1.1. Introduction

Microinverters and power optimizers are widely utilized in modern solar panels to maximize energy efficiency and conversion. Such topologies and implementations usually require a minimum of 25 years of lifetime, which is becoming a critical challenge for market adoption. Low-voltage gallium nitride (GaN) power devices (V_{DS} rating < 200 V) are a promising solution and are being used extensively by an increasing number of solar manufacturers.

In this section, a test-to-fail approach is adopted and applied to investigate the intrinsic underlying wear-out mechanisms of GaN transistors. The study enables the development of physics-based lifetime models that can accurately project the lifetimes under the unique demands of various mission profiles in solar applications.

4.1.2. Trends In Photovoltaic Power Conversion

The ever-increasing demand for renewable energy sources has led to a rapid growth in rooftop solar installations across residential and commercial sectors. Traditionally, string inverters have been widely employed in solar installations, where multiple solar panels are connected in series. The inverter is responsible for converting direct current (DC) output from solar panels to alternating current (AC) electricity that can be used to power homes.

String inverters have served as a reliable choice for years. However, they also face many challenges, including reduced performance due to shading, panel mismatch issues, and a lack of module-level monitoring. Most importantly, due to the series configuration of the string inverters, the lowest performing panel dominates the energy conversion rate of the entire system, which could significantly lower the system efficiency.

The Department of Energy released the $1/watt photovoltaic (PV) system initiative in 2010, where developing higher efficiency and more reliable module-level integrated inverters was highlighted as the key area of improvement to meet the target [57]. The SunShot 2030 PV program envisions a similar cost target by 2030 [58]. To meet the goals and maximize energy production, emerging technologies such as microinverters and power optimizers have gained significant attention.

Microinverters are small, individual inverters that are attached to each solar panel, allowing for DC to AC power conversion at the panel level. This enables each solar panel to function at its peak performance by using independent maximum power point tracking (MPPT). Even if a tree branch shades certain panels, all the neighboring panels can still convert at their full capacity. The drop in efficiency only affects the panels in the shade.

Independent tracking also allows solar users to monitor the health of each panel easily. If a panel requires repair, it won't bring down the whole system. In addition, microinverters make it easy to add panels to increase power output. Microinverters can be more expensive than string inverters but can pay off over time by getting more power from your system. Therefore, microinverters in the market need to match panel guarantees with 25-year warranties [59,60].

Power optimizers are DC-DC converters integrated into the solar panel wiring, enabling MPPT of each individual solar panel by continually regulating the dc characteristics to maximize energy output. A power optimizer is a good solution for situations where shading is an issue, or the panels must be placed on multiple roof surfaces with different orientations. Therefore, power optimizers generally are a more energy efficient solution than string inverters. The power optimizer also requires 25 years of warranty [61,620].

4.1.3. Applying Test-to-Fail for Solar

After reviewing the benefits that are driving the switch from string inverters to microinverters and power optimizers in photovoltaic systems, the test-to-fail methodology is introduced and the three device "stressors" most likely responsible for device failure are identified—gate bias, drain bias and temperature cycling. In the subsequent sections, the impact of each of these factors on device lifetime, expressed in terms of mean time to failure (MTTF) and other parameters, is assessed.

To address the reliability concerns surrounding the requirement for 25 years of reliable operation, a test-to-fail approach [4,9,70,73] is adopted and applied to GaN devices that are commonly used in solar applications.

By understanding the underlying failure mechanisms, physics-based lifetime models are developed to explain the unique characteristics of GaN. The developed models can be used to accurately project the lifetimes under all mission profiles that are unique to solar applications.

By examining the mission profiles for solar applications, three key reliability stressors are identified; gate bias, drain bias and temperature cycling (TC). The total MTTF can be described by Equation 4-1.

$$\frac{1}{MTTF_{Total}} = \frac{1}{MTTF_{Gate}} + \frac{1}{MTTF_{Drain}} + \frac{1}{MTTF_{TC}} \quad \text{Eq. 4-1}$$

Therefore, it is critical to understand which stressor is the limiting factor in reliability. This stressor warrants more consideration during design and operation.

4.1.4. Gate Bias

GaN high electron mobility transistors (HEMTs) are used in dc-ac (microinverters) or DC-DC (power optimizers) topologies in their solar applications. The gate terminal must be biased periodically during switching. Hence, gate reliability over time is the first stressor to examine. As shown in Figure 3-2 (Section 3.1.2), GaN HEMTs have an approximately 1-ppm failure rate projected after 25 years of continuous DC bias at $V_{GS(max)}$ = 6 V.

4.1.5. Drain Bias

The low on-resistance ($R_{DS(on)}$) and small die size of GaN HEMTs significantly increase the power conversion efficiency and reduce the power losses in microinverter and DC-DC converter applications. However, one common concern for GaN is dynamic on-resistance.

The flyback is one of the more popular topologies for microinverters in solar applications. When selecting the appropriate GaN transistors for the primary side, three main contributing factors to the drain voltage are considered. These are (1) the bus voltage, (2) the flyback voltage, and (3) the voltage overshoot due to ringing caused by the parasitic inductance in the design. The typical bus voltage for a microinverter is 60 V in a solar application. The flyback voltage is determined by the product of the system's output voltage and the turns ratio of the transformer. By adding some margin for the voltage overshoot and derating, a 170-V maximum V_{DS} rating is frequently desired by the solar customers using such topology.

The EPC2059 [63] is a 170-V maximum V_{DS} rated product that meets the general requirements for microinverters in solar applications. Fig. 4-1 shows the in-situ $R_{DS(on)}$ test results of a representative EPC2059 device that was operated under continuous hard switching at 136 V (80% of the max rated drain bias of 170 V) while the case temperature was modulated at 80°C. This temperature is used because it is considered the nominal operating temperature for solar panels. As shown in Fig. 4-1, the lifetime model is plotted against the measured data. The model predicts the $R_{DS(on)}$ increase due to continuous hard switching in 25 years to be approximately 10%.

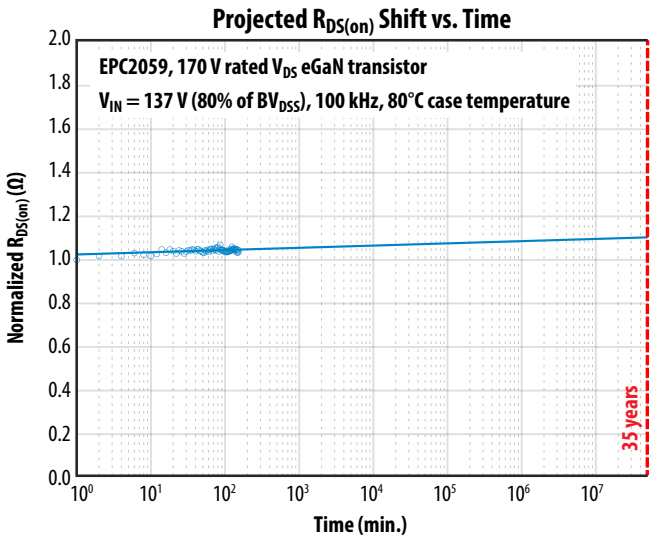


Fig. 4-1. The projected $R_{DS(on)}$ shift of the EPC2059, a 170-V rated device, in 25 years of 100-kHz continuous hard-switching operation at 136 V is approximately 10%. The blue circles represent measured data.

Another popular option for solar systems is to use a DC-DC converter in a power optimizer. This has been adopted by many solar providers due to its superior efficiency. EPC's GaN devices such as the 100-V rated EPC2218 [64] and EPC2302 [81] among others, are good fits for this application.

Fig. 4-2 plots the results obtained with the lifetime model alongside the in-situ measured data for two representative devices—the EPC2218 and EPC2302. A shift of less than 10% in 25 years of continuous hard switching at 80% of the max rated drain bias and 100 kHz is expected. This result suggests that dynamic $R_{DS(on)}$ failure is not the dominant factor determining the lifetime for EPC's GaN devices in solar applications.

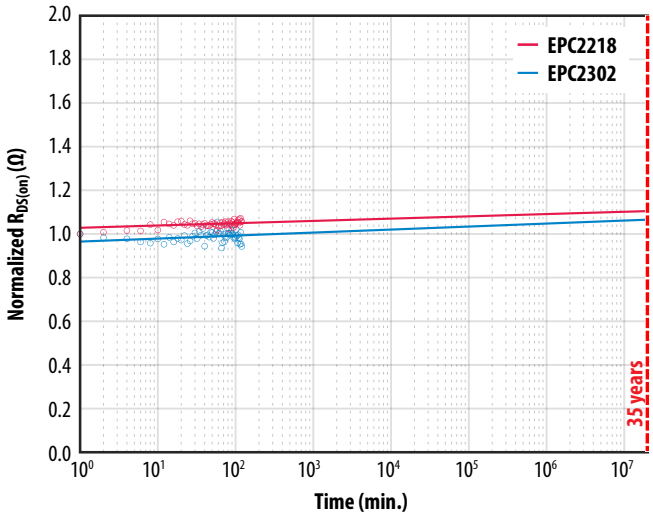


Fig. 4-2. The projected $R_{DS(on)}$ shifts of the EPC2218 and the EPC2302, which both are 100-V rated devices, under continuous hard-switching operation at 80 V, 100 kHz are plotted here. The blue and red circles represent measured data.

4.1.6. Temperature Cycling

Temperature cycling is another critical area of particular interest for solar applications. Solar panels are placed outside, and experience significant ambient temperature changes each day. Therefore, devices mounted on the PCBs in the solar panels must be capable of surviving 25 years of continuous ambient temperature change.

In real world applications, solar panels experience varying ambient temperatures, and the amount of temperature change varies significantly depending on the season and location. As a result, a more-general lifetime model for thermo-mechanical stress is warranted to account for all mission profiles over the 25 years of lifetime. Another TC lifetime model is developed below to account for different ΔT at different seasons of the year, as shown in Equation 4-2.

$$\frac{1}{N_{Total}} = \frac{a}{N_{\Delta T_a}} + \frac{b}{N_{\Delta T_b}} + \cdots + \frac{i}{N_{\Delta T_i}} \qquad \text{Eq. 4-2}$$

where N_{Total} is the total calculated lifetime number of cycles, $N_{\Delta T_a}$ corresponds to cycles-to-failure for the condition of ΔT_a and a is the fraction of time the device was operational under the condition of ΔT_a, $N_{\Delta T_b}$ corresponds to cycles-to-failure for the condition of ΔT_b and b is the fraction of time the device was operational under ΔT_b, and $N_{\Delta T_i}$ corresponds to cycles-to-failure for the condition of ΔT_i and i is the fraction of time the device was operational under ΔT_i.

There are three main factors that predominantly determine the lifetime of the solder joints:

1. The duration of each mission profile needs to be separated. This effect is accounted for by the fractional coefficient in the numerator of each term in equation (4-2), such as a, b, …, and i.
2. The temperature change (ΔT) in each mission profile. This term is addressed by the Norris-Landzberg model plotted in Fig. 4-3. The solder joints experience the most stress during the period when the devices are subjected to the largest ΔT, which translates to the shortest cycles-to-failure. The overall lifetime of the device essentially will be dominated by the most stressful period. This effect is addressed by putting the cycles-to-failure terms ($N_{\Delta T}$) in the denominator and then summing them up collectively.
3. The hottest temperature extreme of each cycle. For instance, the solder joints may experience different stress levels given an identical ΔT in the winter or in the summer.

Each of these factors is included in the analysis that follows, which is based on the board-level thermomechanical reliability study presented in Section 3.4.4, assuming a 0.1% failure rate for the EPC2218A with underfill.

The projected lifetime curves using the Norris-Landzberg model are plotted in Fig. 4-3 assuming T_{Max} is 125°C, the worst-case scenario. The horizontal, black-dashed line at 9,125 cycles represents a duration of 25 years of continuous operation assuming one thermal cycle per day.

Fig. 4-3 shows that after 25 years of continuous operation under a constant temperature swing of 72°C from hot to cold, or vice versa, only 0.1% of the EPC2218A devices with underfill material would fail the datasheet limit due to an increase in $R_{DS(on)}$ value. At a 1% failure rate, 99% of the devices should be capable of surviving 25 years of continuous operation when subjected to a constant ΔT of 95°C. Even without underfill material, 99% of the parts should survive a fixed ΔT of approximately 51°C over 25 years of lifetime.

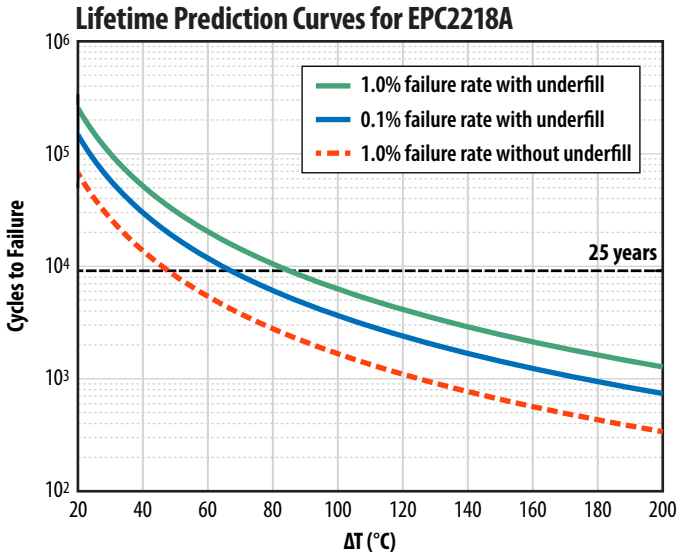


Fig. 4-3. Lifetime prediction curves for EPC2218A with respect to ΔT using the Norris-Landzberg model

Now let us examine a real-world example of the lifetime model from Equation 3-19 (Section 3.4.4). Assume that system is installed outdoors near solar panels in Phoenix, Arizona, U.S.A., where the climate is well-suited for solar, but also demands extreme temperature changes over time. Use the weather report history of Phoenix, Arizona as an example [65].

In addition, 30°C of device self-heating is added to the ambient temperature change for the total lifetime calculations. For the 0.01% failure rate, or 100 ppm, which means 100 devices failed in 1 million parts tested, the EPC2218A with underfill is projected to have 18,218 cycles to failure, equivalent to 49.9 years of lifetime operation considering one cycle per day for GaN devices in the example application.

If we extrapolate to a 0.001% failure rate, or 10 ppm, suggesting only 10 failures out of 1 million devices tested, now the total lifetime is calculated to be 10,971 cycles. This is equivalent to approximately 30 years of continuous operation with one cycle per day.

The results imply that temperature cycling is the most critical stressor that could be limiting the overall lifetime for GaN used in solar applications. However, by using proper underfill materials TC reliability can be significantly improved to exceed the required 25 years of continuous operation with a low failure rate under nominal solar mission profiles.

4.1.7. Conclusions

The test-to-fail results and physics-based lifetime projections show that neither gate bias nor drain bias are major reliability concerns for microinverters or power optimizers in solar applications. Using appropriate underfill materials can vastly reduce thermal cycling reliability risk, resulting in lifetimes exceeding 25 years.

4.2. DC-DC Application Specific Reliability

4.2.1. Introduction

DC-DC converters exist in virtually every application of modern power electronics. Due to small die size, low on-resistance, and low parasitic capacitance, GaN power devices offer superior conversion efficiency and record-setting power density. In this paper, test-to-fail methodology is adopted to investigate the intrinsic wear-out mechanisms such as would be experienced in common DC-DC converters. Devices are stressed under gate bias, drain bias, and temperature cycling individually. The lifetime of each stressor is therefore projected based on the physics-based model developed from test-to-fail and an understanding of the unique stress conditions in DC-DC converters.

GaN devices have demonstrated better switching performance and power density with figures of merit (FOM) 3 to 10 times superior to comparable silicon devices. This trend will only accelerate as GaN FETs continue to improve while Si MOSFET are already very close to their theoretical limits.

GaN devices have enabled easy to use topologies like the synchronous buck converter to reach new levels of efficiency and power densities. Taking advantage of reduced switching losses and no reverse recovery, designers can increase switching frequencies while also reducing power losses. This increase in switching frequency allows for smaller, more efficient inductors that in turn can increase efficiencies by further lowering resistive losses while reducing overall volume. The amount of capacitance can also be cost reduced and with better transient response. Overall, this leads to designs with higher power density, higher efficiency, and lower system cost, hence the broad adoption trends seen throughout various end markets.

GaN HEMTs are particularly valuable where power density is the goal. For example, designers have taken advantage of EPC wafer level chip scale packaging (WLCSP) to significantly increase the power density of intermediate bus converters (IBC) for server applications migrating to a 48V distribution rail. Many designers have chosen an LLC topology operated as DC transformer (DCX) with GaN in both primary and secondary sides. On the primary side the small size of GaN allows the devices to reduce conduction and gate drive losses in the same footprint as a power MOSFET, while the small COSS allows the LLC to operate with a higher power delivery cycle and better transformer utilization. On the secondary side GaN enables the lowest conduction losses in a given area while minimizing gate drive losses thanks to the very small QG. This combination of best-in-class power devices and advanced packaging technologies has allowed for record power densities [66].

4.2.2. Test-to-Fail Methodology

In DC-DC applications, three key stressors are identified; gate bias, drain bias and temperature cycling (TC). The total MTTF can be described by Equation 4-3,

$$\frac{1}{MTTF_{Total}} = \frac{1}{MTTF_{Gate}} + \frac{1}{MTTF_{Drain}} + \frac{1}{MTTF_{TC}} \qquad \text{Eq. 4-3}$$

4.2.3. Gate Bias

In DC-DC converters, the gate terminal of GaN HEMTs must be biased periodically during switching. GaN HEMTs have approximately 1 ppm failure rate projected after 25 years of continuous DC bias at $V_{GS(max)}$ = 6 V. This shows that gate bias stress is not the dominant stressor limiting the overall lifetime.

4.2.4. Drain Bias

A frequently discussed reliability concern for GaN under drain bias is dynamic on-resistance. This is a wear out mechanism where the $R_{DS(on)}$ of GaN HEMTs rises when the devices are subjected to high drain-source voltage (V_{DS}). One of the dominant mechanisms responsible for the increase in $R_{DS(on)}$ is hot electron induced trapping effects [1,5,9,67]. As the trapped charges accumulate, electrons from the 2DEG are depleted, leading to an increase in $R_{DS(on)}$. The detailed lifetime model derivation is discussed in Section 3.2.

The next sections address the following knowledge gaps:

1. How can a representative drain voltage waveform of a common DC-DC converter be correlated with various reliability testing topologies (stressors)?

2. What are the projected lifetimes of each individual reliability testing topology (stressor) based on the lifetime model developed from the electron trapping effect?

3. How does individual reliability lifetime prediction determine the overall lifetime of GaN devices?

First, a SPICE simulation was conducted for a buck converter using an EPC9078 demonstration board featuring 100 V EPC2045 GaN transistors [68]. To include the corner conditions for a real-world application, an intentionally poorly designed buck converter was simulated, where abnormally high parasitic inductances were added to emulate a worst-case scenario [1,5,9]. Figure 4-4(a) shows the simulated turn-off voltage waveform, where the drain voltage immediately rings to a peak voltage of approximately 120 V and then the amplitude of ringing drops off quickly to stabilize at a bus voltage of 80 V. The simulated voltage waveform in Figure 4-4(a) can be deconvoluted by two separate voltage waveforms as shown in Figure 4-4(b) and (c). Figure 4-4(b) illustrates that the overvoltage ringing can be fitted with a set of half-sinusoidal voltage waveforms. After the ringing subdued and reaches the bus voltage, the equilibrium part of the waveform can be modeled by a voltage waveform as shown in Figure 4-4(c). Waveforms in Figure 4-4(b) and (c) can be realized by two different reliability testing circuits, which will be discussed separately in the following discussions.

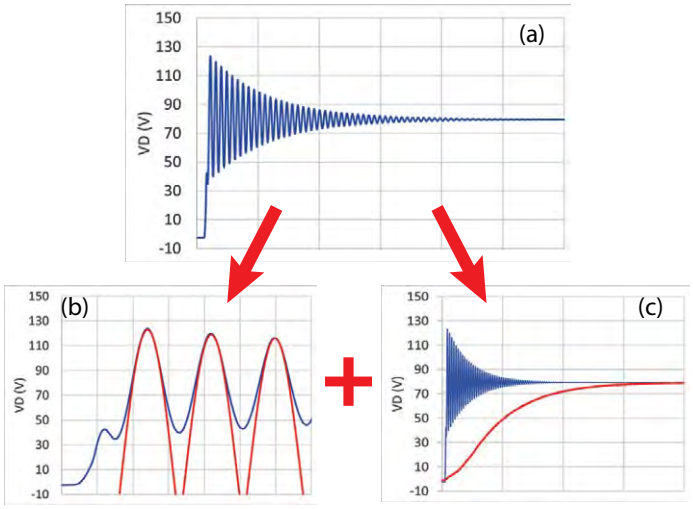


Figure 4-4 (a) A simulated turn-off drain voltage waveform based on a poorly designed buck converter, where a 120 V ringing and 80 V bus voltage are shown. (b) Ringing can be fitted with a set of half-sinusoidal waveforms. (c) The equilibrium portion of the waveform can be fitted by a different voltage waveform shown in red.

Transient overvoltage ringing is commonly observed in GaN HEMTs under high dV/dt switching conditions. Because GaN HEMTs lack avalanche mechanisms, the reliability impact under such transient overvoltage stress is becoming a critical challenge for the industry. To properly address this concern, an unclamped inductive switching (UIS) test circuit was developed as shown in Figure 4-5(a). Figure 4-5(b) shows a half-sinusoidal voltage waveform with a 120 V overvoltage spike that is generated by the UIS test system developed. This transient overvoltage testing was performed at 100 kHz repetitively with a 6% duty cycle during which the GaN HEMT is turned on and $R_{DS(on)}$ is monitored in-situ.

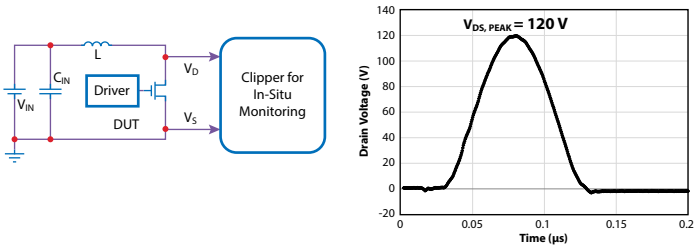


Figure 4-5 (a) Circuit schematic of a UIS test system with a clipper circuit used for in-situ $R_{DS(on)}$ monitoring. (b) a 120 V peak overvoltage drain waveform generated by UIS.

Figure 4-6 (a) shows in-situ measured $R_{DS(on)}$ of three representative EPC2218 devices [64] (100 V rated $V_{DS,Max}$) from three different manufacturing lots under 120 V peak overvoltage testing, 20% more than the datasheet maximum rating. All three devices were tested up to approximately 1.5 billion cycles, where a minimal $R_{DS(on)}$ shift was observed. The case temperature of all three DUTs was maintained at 75°C throughout the experiment by an active temperature control system. Due to the small junction-to-case thermal resistance of 0.5°C/W [64] and very little power dissipation during UIS testing (<0.3 W), the junction temperature of the DUT is virtually identical to the case temperature. As shown in Figure 4-6 (a), the in-situ measured $R_{DS(on)}$ in all cases is well below the datasheet limit scaled by the temperature coefficient (1.35x from 25°C to 75°C) [64]. In addition, the measured data points of each device follow a respective linear trend line in log-t scale on the horizontal axis, validating the lifetime model discussed in Section 3.2. Figure 4-6 (b) shows the 120 V overvoltage testing results of another representative 100 V rated GaN transistor EPC2302 [81] in a power quad flat no-lead (PQFN) package. The DUT was tested to approximately 10 billion cycles at ambient temperature (25°C), where very little $R_{DS(on)}$ shift was seen. A good agreement between 10 billion data points and the lifetime model (blue fit line) was also observed, proving the validity and versatility of the lifetime model. Results presented in Figure 4-6 show excellent overvoltage robustness of GaN HEMTs under 120% of $V_{DS,Max}$.

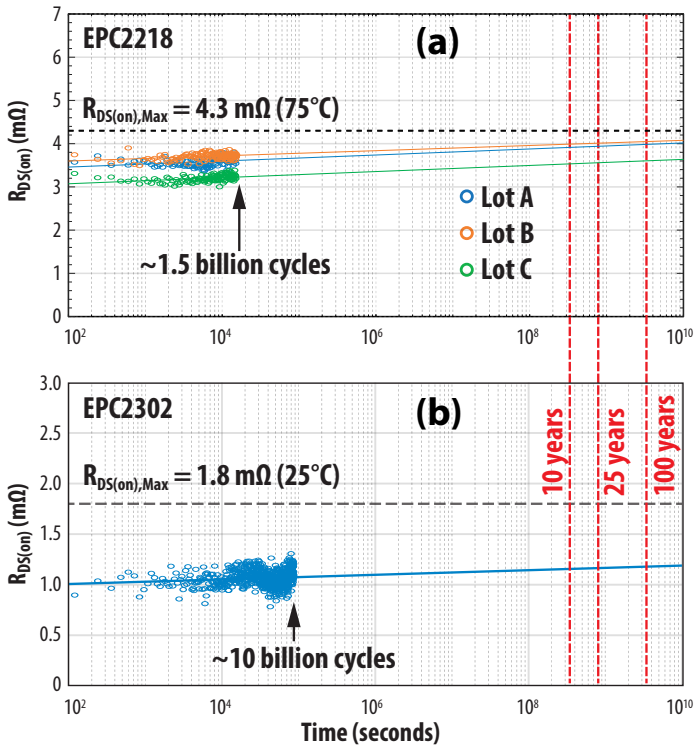


Figure 4-6 (a) In-situ measured $R_{DS(on)}$ from three different EPC2218 lots tested by UIS to 1.5 billion cycles of 120 V overvoltage spikes. (b) In-situ measured $R_{DS(on)}$ of a representative EPC2302 QFN GaN HEMT to 10 billion cycles of 120 V overvoltage spikes.

In a typical turn-off voltage waveform, there are usually multiple overvoltage oscillations before it stabilizes at the bus voltage. However, the first spike typically has the highest voltage. First-principles modeling estimates that the very first overvoltage pulse causes the most trapped charges, which dominates the dynamic $R_{DS(on)}$ shift in every switching period [1,5,9]. Therefore, the dynamic $R_{DS(on)}$ impact resulting from a single overvoltage pulse stress from UIS is representative of the entire ringing portion during a switching period.

Figure 4-4(c) shows how the equilibrium portion of the voltage waveform can be fitted. In Figure 4-7(a), a resistive hard switching topology circuit with in-situ $R_{DS(on}$ monitoring was developed to study the wear-out mechanism involving hot electron trapping during hard switching. Figure 4-7(b) shows that the measured drain voltage rises from zero to the bus voltage (80 V) while the drain current (not presented) drops from the load current (several Amps) to virtually zero (leakage current) simultaneously. This hard-switched topology provides orders of magnitude more hot electrons than the typical high temperature reverse bias (HTRB) reliability testing configuration where the available number of electrons is limited by the low leakage current. The resistive load switching circuit also operates at 100 kHz with 15% duty cycle during which the DUT is on and $R_{DS(on)}$ is measured in-situ. This also means that the DUT is turned off 85% of the time, which is equivalent of 8.5 µs per switching period. Figure 4-7(b) plots the resulting hard switched turn-off voltage waveform that is matching the deconvoluted voltage waveform shown in Figure 4-4(c).

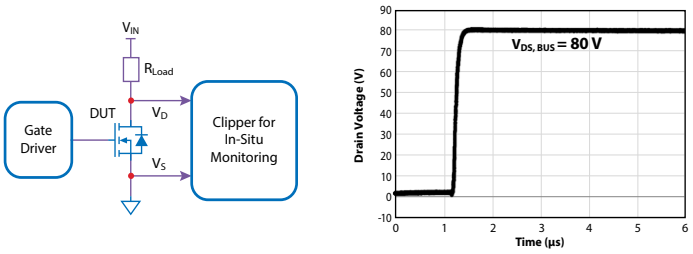


Figure 4-7: (a) Circuit schematic of a resistive load hard switching test system with a clipper circuit used for in-situ $R_{DS(on)}$ monitoring. (b) a turn-off drain voltage waveform to 80 V bus voltage produced by the resistive load hard switching circuit.

Figure 4-8 shows the test results of one representative of EPC2218 and EPC2302 each under 80 V, 100 kHz testing condition. To better view the evolution of $R_{DS(on)}$ drift, all the in-situ measured $R_{DS(on)}$were normalized to the first measured data point and plotted in Figures 4-8 where the vertical axis is normalized $R_{DS(on)}$. Similar to the UIS results, the lifetime model also provides a good fit to the data points collected by the resistive load hard switching test circuit, which further validates the applicability of the lifetime model. The model predicts less than 10% $R_{DS(on)}$ increase over 100 years of continuous switching at 100 kHz and 80 $V_{DS,Bus}$, as shown in Figures 4-8, revealing good robustness of GaN HEMTs under nominal bus voltage hard-switched stress conditions.

Previous work also conclusively demonstrated that this hot electron trapping induced $R_{DS(on)}$ shift has a negative temperature coefficient because of the negative temperature dependence of mean free path discussed in Section 3.2.

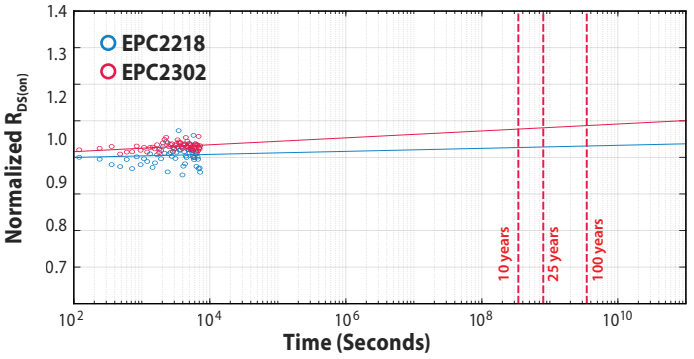


Figure 4-8: The in-situ measured $R_{DS(on)}$ of one EPC2218 and one EPC2302 under 80 V and 100 kHz resistive load had-switched testing conditions, where both devices project less than 10% $R_{DS(on)}$ shift over 25 years of continuous operation.

Using this information, how can the reliability results from two different testing topologies be combined into one that is representative of a real-world DC-DC converter?

Because two different testing topologies address different spectrums of a common turn-off voltage waveform from a buck converter, the reliability impact of each individual stressor can be combined as shown in Equation 4-4, which highlights that the harsher drain bias stressor dominates the overall lifetime.

$$\frac{1}{MTTF_{Total\_Drain}} = \frac{1}{MTTF_{Overvoltage}} + \frac{1}{MTTF_{Bus\ Voltage}} \qquad \text{Eq. 4-4}$$

Previously, 25 years of continuous operation was used as a lifetime projection target used in Figures 4-6 and 4-8 for general DC-DC converter applications. However, the projected $R_{DS(on)}$ values at the end of 25 years are still notably less than the datasheet maximum limit in both cases.

Figure 4-9 shows the projected time-to-failure for EPC2218 under UIS (120 V $V_{DS,Peak}$) and resistive load hard switching (80 $V_{DS,Bus}$) is $8x10^{10}$ seconds and $4x10^{15}$ seconds, respectively. By plugging the time-of-failure results into Equation 4-4, the total lifetime is dominated by the overvoltage contribution because it is orders of magnitude less than the resistive load switching testing result. The total lifetime is calculated to be approximately 2,570 years, which is based on 100 kHz testing data. If designers need to scale the projected results to the actual operating frequency, a simple frequency ratio can be applied to adjust the lifetime as discussed earlier, where 1 MHz operating frequency would yield 257 years of equivalent lifetime.

The projected total lifetime results show that even under an extreme drain bias condition caused by a buck converter with severe overshoot, GaN HEMTs still demonstrated excellent robustness. In

summary, dynamic on-resistance wear out mechanism should not be a critical concern for EPC's GaN HEMTs for use in common DC-DC converters.

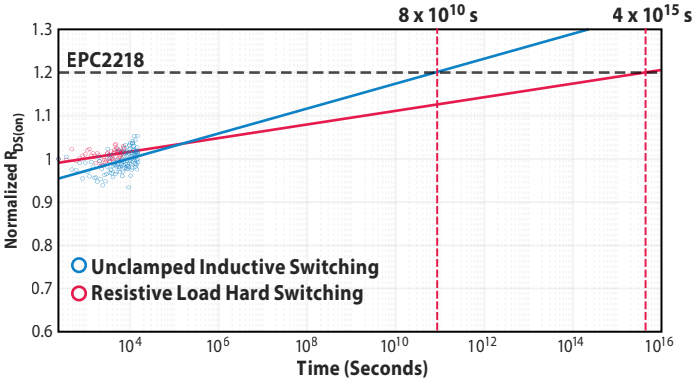


Figure 4-9: Normalized $R_{DS(on)}$ of two EPC2218 devices were projected to a time where $R_{DS(on)}$ shifts 20% as compared to first read point. One EPC2218 device was tested by UIS test circuit. The other one was tested by the resistive load hard switching circuit.

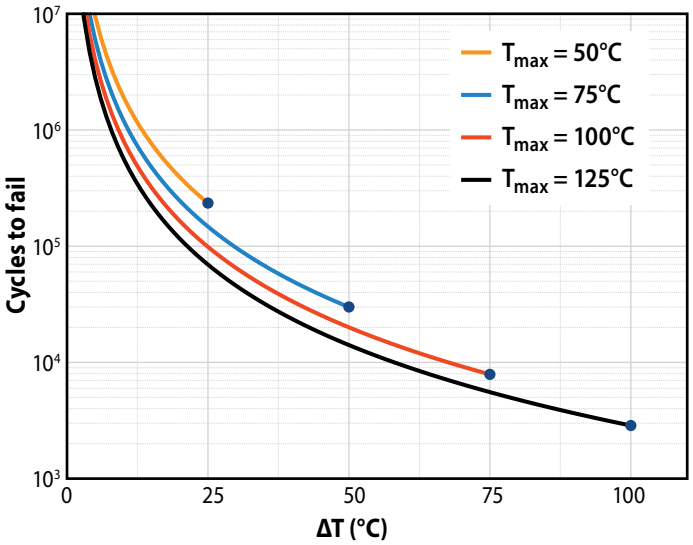


Figure 4-10: Number of cycles to fail at 100 ppm or 0.01% failure rate vs. ΔT at T_{Max} of 50°C (yellow), 75°C (blue), 100°C (red), and 125°C (black)

4.2.5. Temperature Cycling

Temperature cycling is another critical area of interest for DC-DC converter applications.

This analysis is based on the board-level thermomechanical reliability study presented in Section 3.4.4, which showed that proper underfill material improves the temperature cycling lifetime of CSP GaN devices by a factor of at least 4.8x. In the following discussions, only TC1 with underfill data is used.

For an upper limit in this analysis, T_{Max} is assumed to be 125°C, which is the typical maximum design temperature for power modules. The number of cycles to failure (N) at 100 ppm, or 0.01%, failure rate for EPC2218A with underfill can be plotted as a function of ΔT using Equation 3-19 (Section 3.4.4), while the Arrhenius term is a constant coefficient. The result is shown by the black line in Figure 4-10. The horizontal axis (ΔT) only includes a range of 0 to 100°C because power modules in real-world applications are typically kept at 25°C ambient temperature when not in operation, which yields a maximum ΔT of 100°C.

In some of the DC-DC converters that are designed for a lower T_{Max} of 100°C during normal operation, the Arrhenius term should now be slightly larger due to a smaller denominator (T_{Max}) in the exponential equation. The red line in Figure 4-10 shows the number of cycles to fail at 100 ppm extracted from the Weibull distribution as a function of ΔT, where the red curve is slightly above the black curve (T_{Max} = 125°C). Because T_{Max} is lowered by 25°C, the red curve is now plotted from 0°C to 75°C on the horizontal ΔT axis.

For some applications that are designed for a T_{Max} of 75°C, the model is plotted in blue, where a longer lifetime is expected because of the larger Arrhenius term. A T_{Max} of 50°C is also included in Figure 1, as shown in the yellow line.

How can designers use Figure 4-10 to determine the TC lifetime for their DC-DC converter design?

By way of example, take a converter that will be operating in the desert climate of Phoenix, AZ, USA. The ambient outside temperature in the summer can be as high as 50°C (122°F). This notional converter generates another 75°C of heat during operation, which gives a T_{Max} of 125°C. By following the black curve in Figure 4-10 and finding the vertical intercept where ΔT of the horizontal axis is 75°C, the estimated number of cycles to 100 ppm failure rate is a little more than 5000 cycles, hopefully representing decades of operation when also considering the more moderate temperature seasons. This approach provides a practical method to correlate lab generated TC reliability results to real-world applications.

4.2.6. Conclusions

After reviewing the common stresses experienced by DC-DC converters, a test-to-fail approach was adopted and applied to investigate the intrinsic underlying wear-out mechanisms of GaN HEMTs. Three stressors that are most likely responsible for device failures are identified, which are gate bias, drain bias and temperature cycling. 1 ppm failure rate was projected after 25 years of continuous DC gate bias at the maximum rated voltage (V_{GS} = 6 V). The measured data and the lifetime model predict that the $R_{DS(on)}$ shift is expected to be less than 20% over the lifetime of the part. The wear-out mechanism responsible for temperature cycling (TC) failure is solder joint cracking. A third lifetime model that includes TC range, temperature extreme, and cycling speed was introduced. Combining the wear-out rates of all three stressors shows that neither gate bias nor drain bias is of significant reliability concern in DC-DC converter applications. Thermo-mechanical stress due to TC is deemed to

have the highest risk that warrants careful considerations. Using appropriate underfill materials can vastly reduce TC reliability risk while giving excellent lifetimes.

4.3. Lidar Application Reliability

4.3.1. Introduction to Lidar Reliability

Compared to other applications, GaN FETs used for light detection & ranging (lidar) are often subject to long durations of reverse bias and short pulses of relatively high current. This section evaluates the reliability of devices used in lidar applications, both discrete FETs and GaN lidar ICs which include low-voltage driver circuits.

4.3.2. Long-Term Stability Under High Current Pulses

Compared to other applications, GaN FETs used for light detection & ranging (lidar) are often subject to long durations of reverse bias and short pulses of relatively high current. This section evaluates the reliability of devices used in lidar applications, both discrete FETs and GaN lidar ICs which include low-voltage driver circuits.

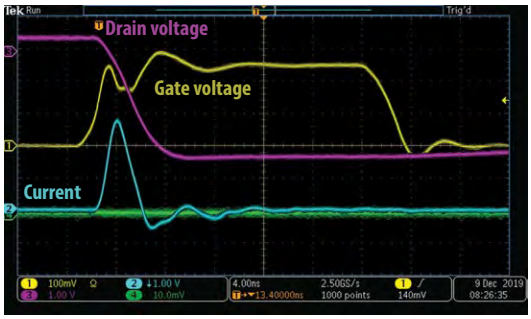
The concept of this test method is to stress parts in an actual lidar circuit for a total number of pulses well beyond their ultimate mission profile. The mission profiles for automotive lidar vary from customer to customer. A typical automotive profile would call for a 15-year life, with two hours of operation per day, at 100 kHz pulse repetition frequency (PRF). This corresponds to approximately four trillion total lidar pulses. Some worst-case (heavy use) scenarios might call for as many as 10–12 trillion pulses in service life.

By testing a population of devices well beyond the end of their full mission profile while verifying the stability of the system performance and the device characteristics, this test method directly establishes the suitability of eGaN devices for lidar applications. To achieve the large number of pulses, parts are stressed continuously, rather than in bursts as used in typical lidar circuits.

For this study, two popular AEC grade parts were put under test: EPC2202 (80 V) [71] and EPC2212 (100 V) [72]. Four parts of each type were tested simultaneously. During the stress, two key parameters were continuously monitored on every device: (1) peak pulse current and (2) pulse width. These parameters are both critical to the range and resolution of a lidar system.

Figures 4-11 and 4-12 show the results of this test over the first 13 trillion pulses. The cumulative number of pulses well exceeds a typical automotive lifetime and covers worst-case use conditions. Note that there is no observed degradation or drift in either the pulse width or height. While this is an indirect monitor of the health of the GaN device, it indicates that no degradation mechanisms have occurred that would adversely impact lidar performance.

These results demonstrate the excellent stability of GaN FETs in lidar applications.



AEC-Q101 series of discrete FETs

- 8 samples (>7000h)
- 0 failures and perfect pulse stability

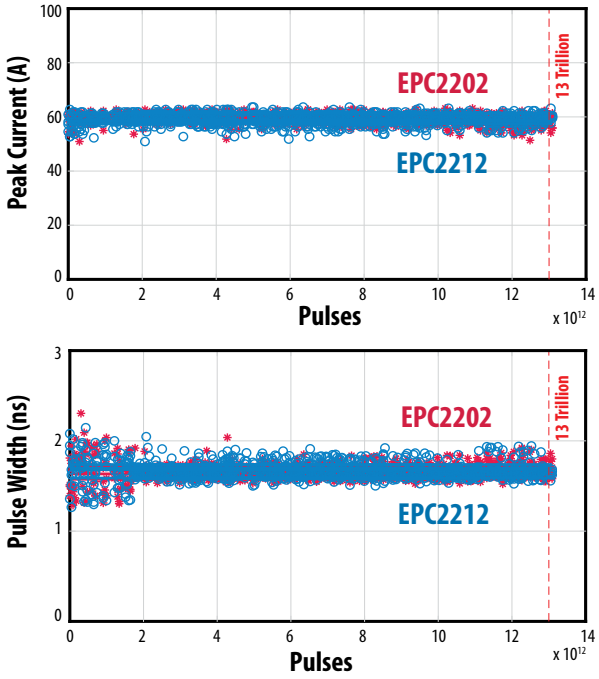


Figure 4-11: Long-term stability of pulse width (bottom) and pulse height (middle) over 13-trillion lidar pulses. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots.

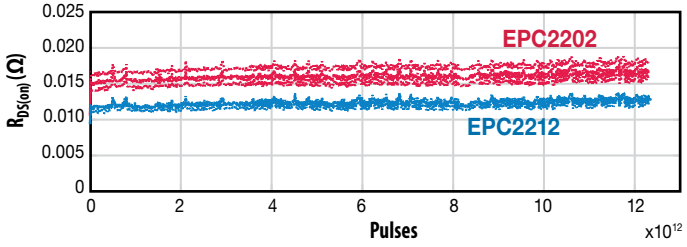


Figure 4-12: Long-term stability of $R_{DS(on)}$ during lidar reliability testing. These parameters are measured at six-hour intervals on every part by briefly interrupting the lidar stress. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots.

4.3.3. Monolithic GaN-on-Si Laser Driver ICs

Lidar systems often use discrete eGaN transistors separate from a gate driver chip due to the benefits of GaN's small footprint and superior switching performance. EPC recently introduced a family of GaN laser drive IC products that integrate a high-speed GaN driver with the discrete GaN transistor , as shown in Figure 4-13. This integrated monolithic lidar solution offers even higher performance, smaller form factor, and lower cost than the existing discrete solutions. As a result, these ICs enable a wider range of lidar applications including robotics, surveillance systems, drones, autonomous cars, vacuum cleaners, and many more.

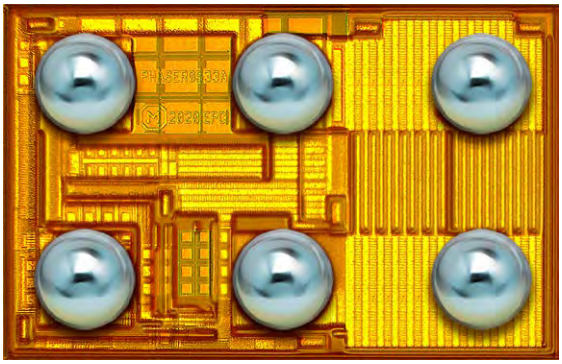


Figure 4-13: The EPC21601 eToF™ integrated circuit includes a driver and a power FET.

The first two offerings of the integrated GaN laser drive IC products (EPC21601 [74] and EPC21701) [75] are in production. Table 4-1 summarizes the main specifications of the first two qualified IC products.

Part Number	Die Size (mm x mm)	Main Specifications
EPC21601	S (1.5 X 1)	40 V, 15 A, 3.3 V logic, eToF laser driver IC
EPC21701	S (1.7 X 1)	80 V, 15 A, 3.3 V logic, eToF laser driver IC

Table 4-1: Initial EPC Laser Driver IC Product Family

4.3.4. Key Stressors of eToF Laser Driver IC for Lidar Application

The integration of the gate driver and power transistor into a chip-scale package greatly reduces the parasitic inductances and further improves the speed, minimum pulse width and power dissipation. It also introduces challenges in isolating the key electrical stressors because many of the IC's voltages and currents cannot be accessed directly. The first step of the study is to identify the key stressors that affect the IC in lidar applications.

Both EPC21601 and EPC21701 are selling in a chip-scale BGA form factor that measure at 1.5 x 1.0 mm and 1.7 x 1.0 mm, respectively.

The package technology of the laser driver ICs has been used in EPC's discrete power transistors for many years, and therefore the package related reliability of the IC products was covered by previous phase reliability testing reports and related publications [5,9,15,69-73].

The lidar IC's operating conditions, shown in Figure 4-14, are best emulated through High Temperature Operating Life (HTOL) testing. EPC21601 is selected as the test vehicle for this test-to-fail study.

Three key stressors are identified:

- Logic supply voltage V_{DD} that supplies the drive voltage to the low voltage (LV) GaN FETs in laser driver circuit as well as the gate of the high voltage (HV) GaN output FET.
- Laser drive voltage V_D that is predominantly applied to the drain terminal of the HV output FET.
- Operating frequency which stresses both the LV laser driver circuits and the HV output FET.

4.3.5. Effect of V_{DD}, Logic Supply Voltage

When EPC21601 is operated and generates a burst of short pulses, the logic supply voltage (V_{DD}) is applied to the gate terminals of the LV GaN FETs in the laser driver circuits and the gate of the HV GaN power transistor. It is equivalent of performing a dynamic gate test for all GaN FETs with a burst frequency of 1 kHz, very low duty cycle (~0.02%), and high operating frequency (30 MHz). When not pulsed, the part is in the OFF state and the gate bias is nearly zero (see Figure 4-15).

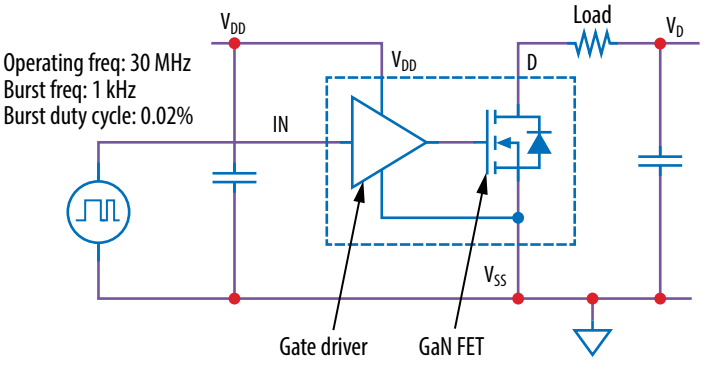


Figure 4-14: Block diagram of EPC21601 and EPC21701 laser drive integrated circuits

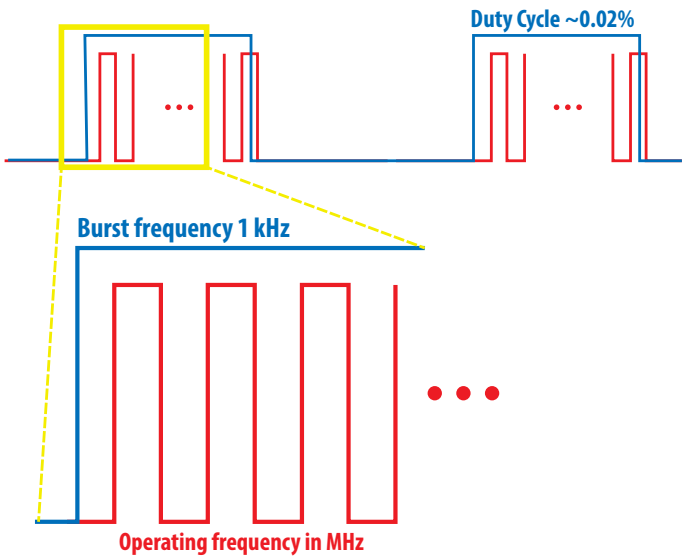


Figure 4-15: Diagram of operating conditions with Burst Frequency (Blue) 1 kHz with a duty cycle of ~0.02% and Operating Frequency in MHz

In the qualification HTOL test, V_{DD} was biased at the absolute maximum rating of 5.5 V, and no issue was found after 1000 hours of testing at 125°C junction temperature. To test the device's robustness, the V_{DD} voltage was increased to a high value at 7 V, which is more than 125% of the absolute maximum rating. This stress condition addresses the worst overvoltage ringing issue on the V_{DD} pin during normal operation by customers. Table 4-2 summarizes the test result where 16 devices were tested up to 1049 hours at 7 V V_{DD} and 125°C junction temperature. No failures occurred. This indicates that a significant margin exists in the laser driver IC products.

As there were zero failures, this result does not determine how much margin was designed into the product or to accurately predict the lifetime at a given mission profile for the V_{DD} stressor. Therefore, more stringent stress conditions must be applied to test the devices to failure, where the goal is to fail the parts quickly and conduct failure analysis to understand the underlying failure modes and mechanisms.

To determine the voltage acceleration of the V_{DD} stress, a matrix of tests was conducted from 8.5 V to 9.5 V at 25°C, as shown in Table 4-3. At 8.5 V V_{DD}, a total of three failures were found after more than 1000 hours of testing whereas almost all parts failed within 305 hours at 9.5 V, indicating a significant voltage acceleration.

Temperature acceleration was also studied by conducting HTOL tests at 25°C and 125°C, while the V_{DD} was fixed at 8.5 V. The results are summarized in Table 4-4 where it shows a significant temperature acceleration.

Failure analysis determined that all failures were soft parameter failures in which quiescent current exceeded the 20 mA maximum datasheet limit, with V_{DD} = 5 V and the measurement conducted during the OFF state [74]. Under closer examination, the quiescent current only exceeded datasheet limits when V_D = 20 V was provided. When the quiescent current soft failures were subjected to lidar operation with a V_D of 15 V, the integrity of their pulses was uncompromised. Figure 4-16 shows the waveforms of the input signal (blue) of V_{IN} (the logic input to EC21601) and the corresponding output signals from V_D of the quiescent current failures (green and yellow), where no pulse distortion or missing pulses were observed. This suggests even when the device was damaged by extremely high V_{DD} stress, it still was functional, and the repeatability of current pulses was not adversely impacted.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size	Duration (Hrs)
HTOL	**EPC21601**	**V_{DD} = 7 V, T_J = 125°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3 V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	0	16	1049

Table 4-2: HTOL Test Result of EPC21601 with V_{DD} = 7 V and T_J = 125°C

Stress Test	Part Number	Test Condition	# of Failure	Sample Size	Duration (Hrs)
HTOL	**EPC21601**	**V_{DD} = 8.5 V, T_J = 25°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3 V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	3	16	1049
HTOL	**EPC21601**	**V_{DD} = 9.5 V, T_J = 25°C**, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3 V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	15	16	305

Table 4-3: HTOL Test Result of EPC21601 with V_{DD} = 8.5 V and V_{DD} = 9.5 V, T_J = 25°C

Stress Test	Part Number	Test Condition	# of Failure	Sample Size	Duration (Hrs)
HTOL	EPC21601	**V_{DD} = 8.5 V, T_J = 25°C,** V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3 V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	3	16	1049
HTOL	EPC21601	**V_{DD} = 8.5 V, T_J = 125°C,** V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3 V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	16	16	718

Table 4-4: HTOL Test Result of EPC21601 with T_J = 25°C and T_J = 125°C, V_{DD} = 8.5 V

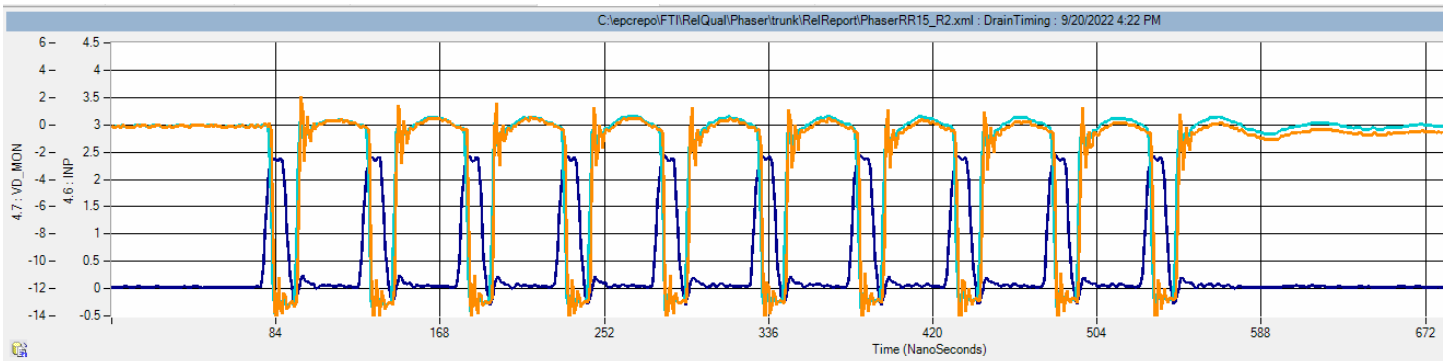


Figure 4-16: The input (blue) waveform and the corresponding output waveforms of the quiescent current failures (green and yellow)

Since all failures at different voltages and temperatures showed similar "soft" electrical failures, physical failure analysis was conducted to determine the underlying root cause. Gate rupture of the LV GaN FETs in the driver circuit was found to be the single failure mechanism for all failures regardless of stress voltages and temperatures. This result is expected based on the circuit analysis because the V_{DD} voltage is applied to the gates of the LV and HV GaN FETs when the pulses are generated.

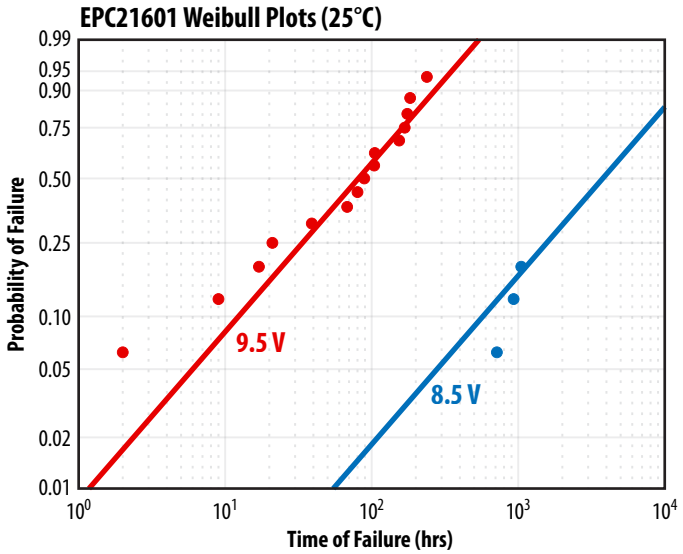


Figure 4-17: Weibull plots showing the failures of EPC21601 at 8.5 V (blue) and 9.5 V (red) V_{DD}, respectively and T_J = 25°C.

Figure 4-17 shows time-to-failure data for the two different V_{DD} voltages at room temperature. The data was analyzed using a two-parameter Weibull distribution for each voltage leg using maximum likelihood estimation (MLE). The fits are indicated by solid lines in the graphs. The Weibull shape (or slope) parameter was constrained to be the same for all voltage legs because a single failure mode was found through failure analysis.

The calculated mean-time-to-failure (MTTF) of the 9.5 V V_{DD} leg is approximately 117 hours, which equals 4.2 X 10^5 seconds. In Figures 1 and 2 of the Phase 14 Reliability Report [5], the MTTF of the 9.5 V V_{GS} DC test of EPC2212 at 25°C is approximately 150 seconds, which is 7.5 x 10^5 seconds when scaling with the 0.02% burst duty cycle that was used in the HTOL test. EPC21601 and EPC2212 share the same gate construction and use identical gate fabrication processes. This shows that static DC V_{GS} testing on EPC2212 and the measured MTTF of EPC21601 in accelerated dynamic gate testing are consistent. It is understandable that the two MTTF values do not match exactly due to the difference in testing setup and implementation. For instance, the gates of all the LV FETs were stressed through the same V_{DD} pin concurrently during an extremely short pulse, where some slight ringing on the gates might be expected. This could explain the slightly worse MTTF for EPC21601 as compared to the DC accelerated gate testing result for EPC2212.

The commensurate MTTF results between EPC21601 and EPC2212 also corroborate the validity of the physics-based model EPC developed for the gate reliability. The same lifetime model fits the measured data for V_{DD} at both biases.

Figure 4-18 shows the lifetime projection against the measured acceleration data for EPC21601 at 25°C. The fit projected greater than 25 years of lifetime with less than 1 ppm failure rate at the 5.5 V maximum V_{DD} voltage rating at 25°C. This result also agrees well with the extrapolated lifetime for gate at 5.5 V under static DC gate bias.

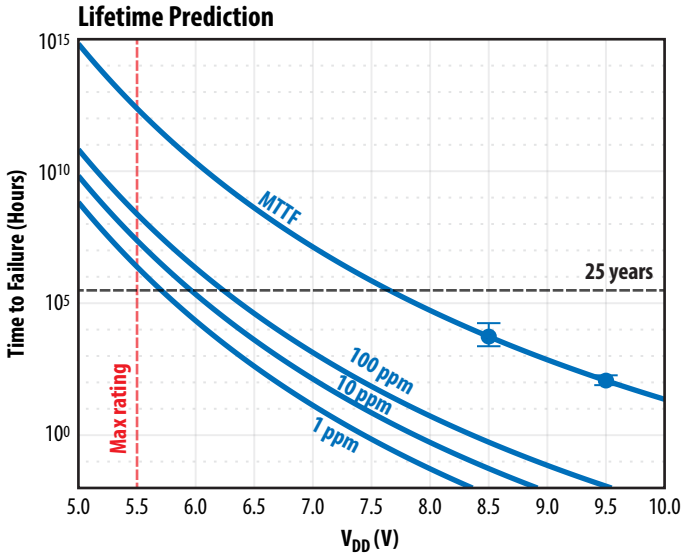


Figure 4-18: EPC21601 MTTF data at two different voltages with error bars are plotted against V_{DD} at 25 °C. The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

Temperature acceleration of the time-to-failure data are shown in Figure 4-19 (25°C and 125°C) while V_{DD} was fixed at 8.5 V. The Weibull shape (or slope) parameter was constrained to be the same for both temperature legs because a single failure mode was identified through failure analysis. The time-to-fail of each device was recorded by conducting a complete ATE post screening after the parts were removed from the oven (125°C leg) and the motherboards. Only the "soft" quiescent current failures were found and summarized in Table 4-4.

Figure 4-20 shows the Arrhenius plot for the MTTF data at 25°C and 125°C with V_{DD} = 8.5 V, where an activation energy of 0.35 eV was calculated by using the Arrhenius equation [92-94]. This result is different from what was observed when conducting static HTGB testing for discrete GaN products, which showed weak negative temperature acceleration. Initial failure analysis showed identical gate rupture as the underlying failure mode for all soft quiescent current failures regardless of 25°C or 125°C testing temperature.

Though the failure mechanism responsible for the temperature acceleration warrants further investigation, the laser driver IC under the V_{DD} stressor is proven to be extraordinarily robust.

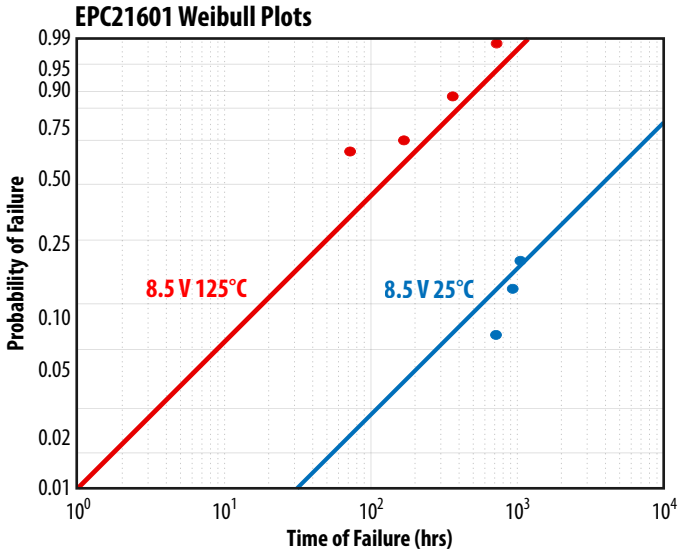


Figure 4-19: Weibull plots showing the failures of EPC21601 at 25°C (blue) and 125°C (red) junction temperature, V_{DD} = 8.5 V.

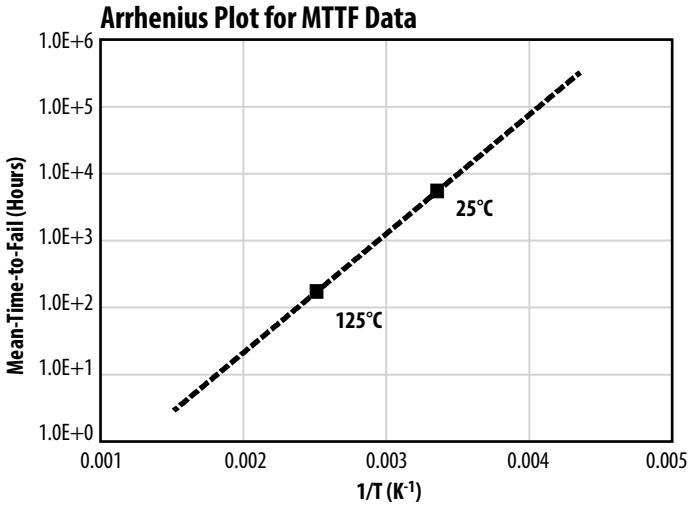


Figure 4-20: EPC21601 MTTF data at two different temperatures are plotted against T^{1} (K^{-1}) with V_{DD} at 8.5 V. The solid line corresponds to the Arrhenius equation, where an activation energy of 0.35 eV was found.

4.3.6. Effect of V_D, Laser Drive Voltage

By examining the circuits that connect to the V_D pin in detail, the accelerated V_D HTOL can cause two potential failure modes in EPC21601.

1. V_D primarily goes to the drain terminal of the HV GaN FET. Due to the nature of lidar operation, the HV output FET is under reverse drain bias most of the time. When the laser pulses are generated, the HV FET turns on and conducts current. Accelerated V_D HTOL testing of the IC therefore resembles a dynamic HTRB test of the output FET with a high duty cycle. Therefore, the intrinsic failure modes due to accelerated drain bias test for a discrete GaN transistor apply.

2. Besides connecting to the drain node of the HV FET, the V_D pin also connects to a single laser driver circuit, which affects the number of pulses generated by the device. If that path was compromised by the accelerated V_D stress, it could lead to missing pulses, which is another crucial failure mode for lidar application.

The HTOL qualification test was conducted at 30 V_D, the maximum recommended voltage specified by the datasheet [74]. A matrix of accelerated V_D HTOL tests were conducted as summarized in Table 4-5. 60 V_D was selected because it is two times of the maximum recommended voltage rating, which is an extremely accelerated condition. However, this voltage shall not be too high to cause some other known intrinsic failure modes for the HV output FET. 60 V is an aggressive test-to-fail condition against the driver design.

Table 4-5 shows that no failures were found after more than 1000 hours of testing. All parts continued to meet the datasheet specifications after undergoing the HTOL tests.

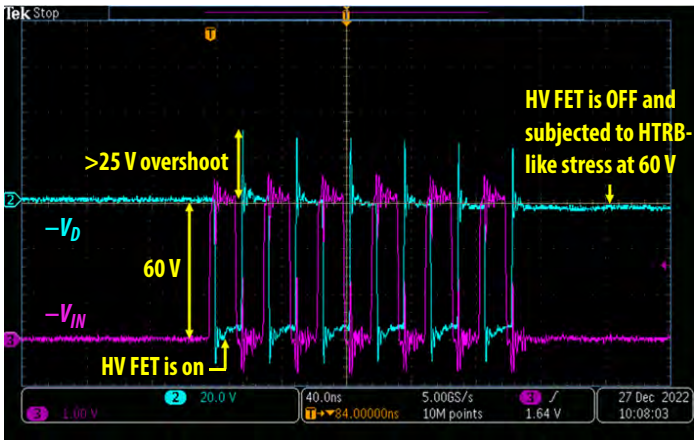


Figure 4-21: Output waveforms (blue) of a representative passing part after it was subjected to 1005 hours of HTOL testing at 60 V V_D and 125°C. The purple waveform is the corresponding input signal from V_{IN}. Please note that a 25 V of overshoot was seen at the end of each pulse during HTOL testing.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size	Duration (Hrs)
HTOL	EPC21601	V_{DD} = 5.5 V, **T_J = 25°C** **V_{D_DC} = 60 V** V_{IN} = 3.3V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	0	16	1005
HTOL	EPC21601	V_{DD} = 5.5 V, **T_J = 125°C** **V_{D_DC} = 60 V** V_{IN} = 3.3V_{P-P}, Burst frequency = 1 kHz; Operating frequency = 30 MHz	0	16	1005

Table 4-5: HTOL Test Result of EPC21601 with V_D = 60 V, T_J = 25°C and T_J = 125°C, respectively

To further validate that the devices were not generating distorted waveforms or missing pulses, the parts from the V_D = 60 V and T_J = 125°C leg were mounted back onto the test setup at 60 V and 125°C and the input and output pulse waveforms were captured as shown in Figure 4-21. This result shows that no degradation in pulse waveforms was observed after more than 1000 hours of HTOL testing. It is also important to note that the HV output transistor experienced more than 25 V overshoot at the end of each pulse during HTOL resulting from the short pulses. It suggests that the device saw repetitive > 85 V transient overvoltage stress (> two times the absolute maximum rating = 40 V) on V_D in addition to the 60 V nominal stress that is another two times the maximum recommended bias. This also demonstrates good robustness of the device under V_D stress.

At this point, the most rigorous testing corner is covered by the testing matrix at the 60 V_D leg at 125°C. Further increasing the drain bias might introduce a different intrinsic failure mechanism for the HV GaN transistor that is not applicable to the lidar application or the reliability of the laser drive IC. In short, no failure mode was found to be associated with the laser supply voltage (V_D).

4.3.7. Effect of Operating Frequency

Preliminary device characterization suggested that the output waveforms of lidar ICs could be distorted when tested at extremely high operating frequencies. It is therefore useful to study at what frequency or duration of the HTOL testing the pulse waveform starts showing significant distortion or missing pulses.

Tests at two high operating frequencies were carried out as shown in Table 4-6. 48 MHz and 96 MHz are 160% and 320% of the 30 MHz maximum recommended operating frequency used in qualification. No failure occurred after more than 1400 hours of testing. All parts continued to meet the datasheet specifications after undergoing the HTOL tests.

Figure 4-22 shows representative input (purple) and output (blue) waveforms of a passing device post 1413 hours of 48 MHz HTOL testing. No waveform distortion or missing pulses were found. Figure 4-23 shows another set of representative input (purple) and output (blue) waveforms of a passing device post 1413 hours of 96 MHz HTOL testing. No waveform distortion or missing pulses were found.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size	Duration (Hrs)
HTOL	**EPC21601**	V_{DD} = 5.5 V, T_J = 25°C, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, Burst frequency = 1 kHz; **Operating frequency = 48 MHz**	0	16	1005
HTOL	**EPC21601**	V_{DD} = 5.5 V, T_J = 25°C, V_{D_DC} = 30 V, R_{LOAD} = 2 Ω V_{IN} = 3.3V_{P-P}, Burst frequency = 1 kHz; **Operating frequency = 96 MHz**	0	16	1005

Table 4-6: HTOL Test Result of EPC21601 with operating frequency of 48 MHz and 96 MHz with V_D = 30 V and T_J = 25°C.

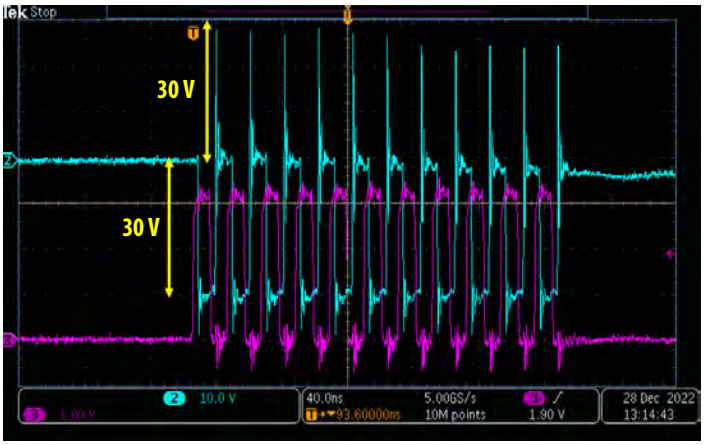


*Figure 4-22: Representative input (purple) and output (blue) waveforms of a passing device after 1413 hours of HTOL testing at **48 MHz** operating frequency. Please note that a 30 V of overshoot was seen at the end of each pulse during HTOL testing.*

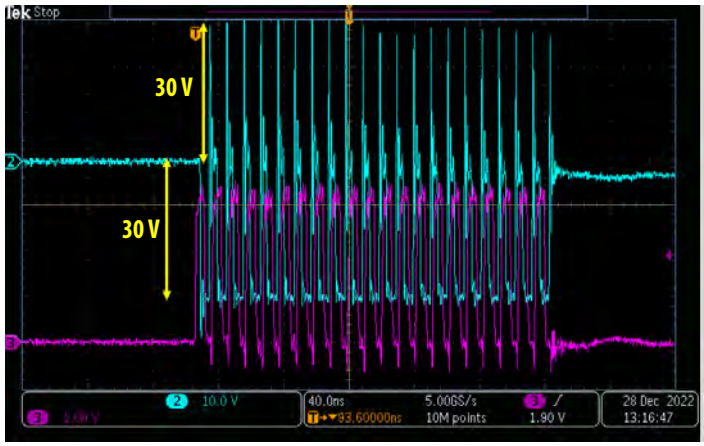


*Figure 4-23: Representative input (purple) and output (blue) waveforms of a passing device after 1413 hours of HTOL testing at **96 MHz** operating frequency. Please note that a 30 V of overshoot was seen at the end of each pulse during HTOL testing.*

So far, no failures of the EPC21601 lidar IC have been generated using input frequency up to nearly 100 MHz HTOL testing for an extended period, which further demonstrates the robustness of the laser driver IC products.

In conclusion, of the three stressors unique to lidar ICs considered in this section – logic supply voltage V_{DD}, laser drive voltage V_D, and operating frequency – only the logic supply voltage was observed to generate device failures. Lidar ICs operated within datasheet limits perform reliably.

5. SUMMARY AND CONCLUSIONS

As GaN device production continues to increase and applications diversify, separate reliability concerns arise which may depend on the use case. By understanding the wear-out mechanisms that affect a system in each phase of its mission profile, GaN device lifetimes can be calculated analytically for each specific application. The failure rate of each wear-out mechanism, which is confirmed by testing to failure, can be minimized by following the guidelines provided in this report.

6. APPENDIX

SOLDER STENCIL DESIGN GUIDELINES FOR RELIABLE ASSEMBLY OF PQFN GAN DEVICES

1. Introduction

Power quad flat no-lead (PQFN) packages have become increasingly popular in power electronics. The solder stand-off height of PQFN packages is intrinsically lower than the traditional ball grid array (BGA) packages. Therefore, it is critical to develop a first-principles stencil design rule that yields consistent solder standoff height with minimum die tilt.

IPC-7525A [76] was the main document used for developing these stencil design guidelines for PQFN devices. By following the design rules, a large number of assembly experiments were conducted and followed with cross-section analysis to quantify the resulting standoff height and component tilt. The cross-sectional results showed consistent planarity of standoff height in all assemblies, validating the effectiveness of stencil designs. Such design rules enable us to predict the standoff height, providing the optimal temperature cycling lifetime.

2. Critical Components of Stencil Design

A combination of aperture dimensions and stencil thickness determines the actual solder paste volume that is deposited to the PCB. A representative cross-sectional view of a stencil is shown in Figure 1. Solder paste fills the stencil aperture during the stencil printing process. When the stencil separates from the PCB, the solder paste is transferred to the PCB with some remaining on the sidewall of the stencil, as illustrated in Figure 2. The aspect ratio and area ratio must meet the minimum requirements specified by the IPC standard [76].

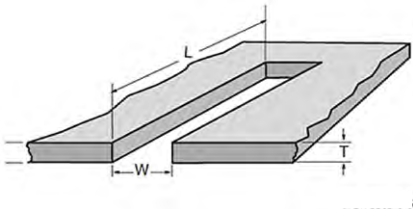


Figure 1: Cross-sectional view of a stencil, where L is the length of the aperture, W is the width of the aperture, and T is the thickness of the stencil.

2.1 Aspect Ratio

Aspect Ratio is the ratio of the aperture's width to the stencil thickness, which is defined by Equation 1. The design rule for acceptable solder paste release is specified to be greater than 1.5. A lower aspect ratio can cause excessive amount of solder paste to stick to the aperture wall during the release process.

$$Aspect\ Ratio = \frac{Width\ of\ Aperture}{Thickness\ of\ Stencil} = \frac{W}{T} \qquad \text{Eq. 1}$$

2.2 Area Ratio

Area ratio is the ratio of the aperture area opening to the total area of the aperture sidewalls, as specified by Equation 2. This is a critical parameter in stencil printing for a better paste release. IPC-7525A specifies that the area ratio should be greater than 0.66.

$$Area\ Ratio = \frac{Area\ of\ Aperture}{Area\ of\ Aperture\ Walls} = \frac{(L \times W)}{2 \times (L+W) \times T} \qquad \text{Eq. 2}$$

2.3 Transfer Efficiency

Transfer efficiency is the ratio between the actual solder volume deposited on the PCB and the total printed solder volume according to the aperture dimensions. Equation 3 defines the transfer efficiency and is further illustrated by Figure 2. There are three main components that determine the transfer efficiency , which are the stencil technology used (laser cut, chemical etching, etc.), aspect ratio, and area ratio.

$$Transfer\ Efficiency\ (\%) = \frac{Volume\ Deposit}{Volume\ Aperture} \times 100\% \qquad \text{Eq. 3}$$

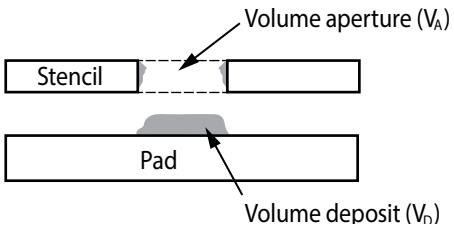


Figure 2: Transfer of Solder Paste onto the pad (Volume deposit). Due to the solder paste adhesion force, some solder paste residue is left on the sidewall of the aperture.

Figure 3 demonstrates that the area ratio significantly impacts the transfer efficiency and repeatability of the solder paste deposit. The data shows that a larger area ratio is preferred, which yields higher transfer efficiency and lower assembly variations.

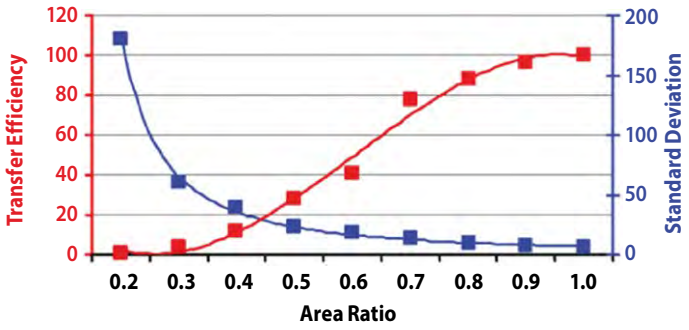


Figure 3: Transfer efficiency vs. area ratio and standard deviation cited from ref. [77].

2.4 Solder Paste Shrinkage

Solder paste mainly consists of two portions, which are solder spheres and flux, as illustrated in Figure 4. After the reflow process, the solder paste would shrink to approximately 50% of the initially deposited volume, equivalent to 85-90% of the weighted percentage [78].

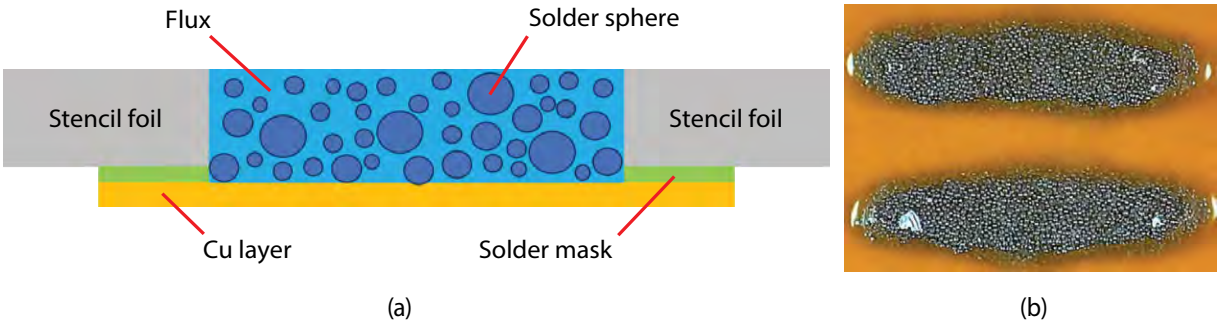


Figure 4 (a) shows the volume of the solder sphere and flux inside the aperture. (b) shows an example of deposited solder paste on the pad after release.

3. Stencil Design Methodology and the Impact on Stand-Off Height (SOH)

PCB land patterns are the exposed copper pads that serve as a connection pathway to the components via solder joints. Solder paste is the only added interconnect medium between the PCB and QFN components. After reflow, the solder joints formed, where the land pattern and stencil opening predominantly determined the shape and dimensions of the solder joints. To develop a design rule, the solder joints of PQFN devices can be generally categorized into four sub-components that will be discussed in the following discussions.

3.1 Solder at Body

Solder at body is defined as the solder portion that exclusively sits beneath the exposed pads, as highlighted by the red box in Figure 5. The entirety of the solder at body contributes to the stand-off height. Therefore, 100% of the solder paste deposited stays in this location.

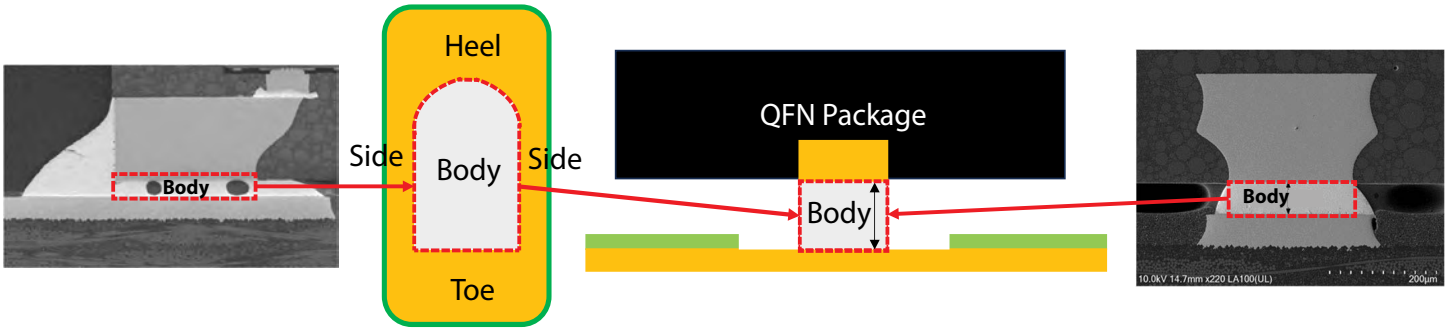


Figure 5: Illustration of the impact of the solder body on stand-off height

3.2 Solder at Side

Sidewall solder fillets are the sides of a triangular solder joint formed after reflow, as illustrated in Figure 6. The triangular shape is because the land patterns are typically larger than the exposed pads. Figure 6 shows that approximately 50% of the solder paste deposited stays at the sides after reflow.

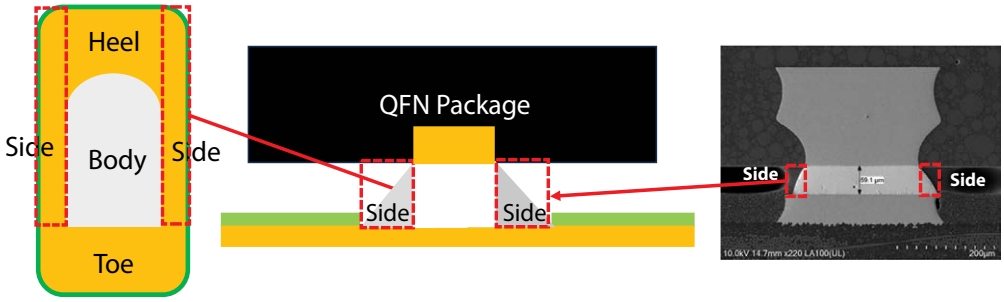


Figure 6: Illustration of the impact of the solder at the side on stand-off height

3.3 Solder at Heel

Heel solder fillet is the inner portion of the solder joint formed after reflow, as shown in Figure 7. The solder at heel contributes to approximately 50% of the solder paste deposited.

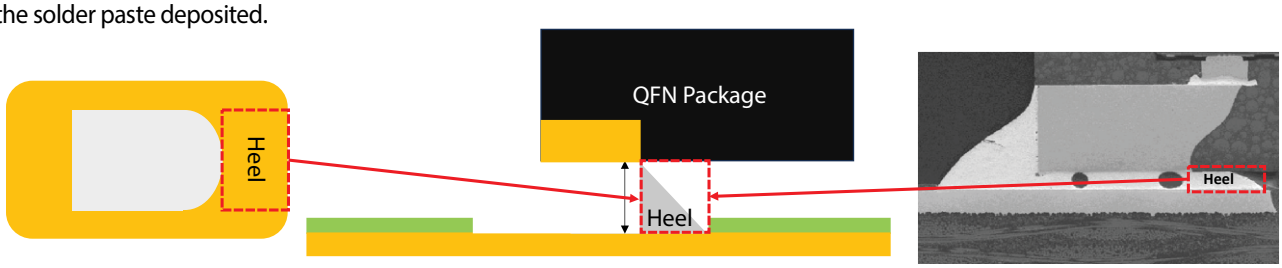


Figure 7: Illustration of the impact of the solder at the heel on stand-off height

3.4 Solder at Toe

Toe solder fillet is the outer portion of the solder joint and stays outside the exposed pads, as illustrated by Figure 8. Hence, the toe fillet does not impact stand-off height. Although it does not directly contribute to the stand-off height, it plays a vital role in determining the fillet height of the sidewall solder connection. The complete wetting of the sidewall wettable flanks leads to the maximum fillet height, which usually improves the mechanical bonding strength of the solder joints and, therefore, better temperature cycling reliability performance [79].

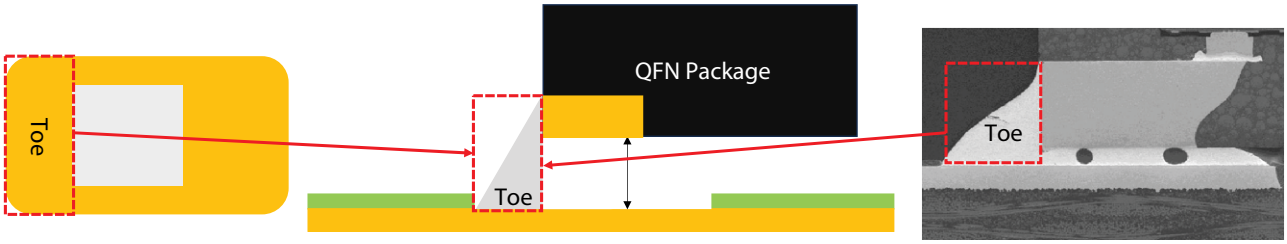


Figure 8: Illustration of the impact of the solder at the toe on stand-off height

3.5 Solder Paste Coefficient Factor (k)

Solder paste coefficient factor is the by-product of solder paste shrinkage and transfer efficiency as discussed in Figure 2–4. Equation 4 further quantifies this parameter.

$$k = solder\ paste\ shrinkage\ \% \times transfer\ efficiency\ \% \qquad \text{Eq.4}$$

Table 1 summarizes the coefficient factors of various shapes of exposed pads with 100 µm and 150 µm thick stencil. The transfer efficiency decreases when increasing the stencil thickness from 100 µm to 150 µm but solder paste shrinkage stays the same.

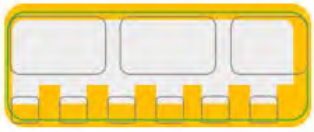
Pad Category	Representative Pad Shape	Coefficient Factor (k) 100 µm Thick Stencil (Shrinkage x Transfer Efficiency)	Coefficient Factor (k) 150 µm Thick Stencil (Shrinkage x Transfer Efficiency)
1. Small Opening		k = 50% · 90% = 45%	k = 50% · 80% = 40%
2. Medium Opening		k = 50% · 100% = 50%	k = 50% · 80% = 40%
3. Big Opening		k = 70% · 100% = 70%	k = 70% · 80% = 56%

Table 1: Coefficient Factor (k) for small, medium, and big pads with 100 µm and 150 µm thick stencils

3.6 Formula of Calculating Stand-Off Height

After transfer and reflow, the deposited solder sphere alloy volume is $A_{aperture} \cdot t \cdot k$, where $A_{aperture}$ is the total area of the solder stencil opening, t is its thickness, and k is the solder paste coefficient. For toe land pattern area A_{toe}, a solder volume of approximately $A_{toe} \cdot t \cdot k$ is used for the solder toe. Solder joint components other than the toe will combine to determine the solder stand-off height based on the remaining deposited solder volume. By this logic, the solder stand-off height (SOH) of each lead can be calculated as shown in Equation 5.

$$SOH = \frac{(A_{aperture} - A_{toe}) \times t \times k}{A_{body} + 0.5A_{sides} + 0.5A_{heel}} \quad \text{Eq.5}$$

where A_{body}, A_{sides}, and A_{heel} are the body, total side, and heel areas, respectively, and the factors of 0.5 are due to the triangular shape of the side and heel solder components.

4. Case Study 1: A 3.5 x 5 mm PQFN IC EPC23102 [80] with 100 µm Thick Stencil

Figure 9 is the die layout of the PQFN IC, EPC23102, and Figure 10 is the stencil design developed by following the design rule as discussed earlier.

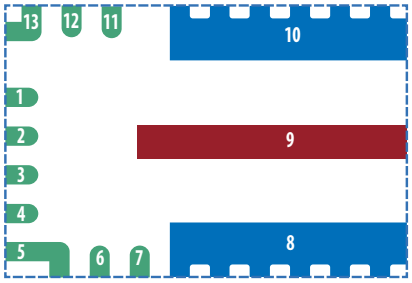


Figure 9: EPC23102 PQFN 3.5 x 5 mm bump layout

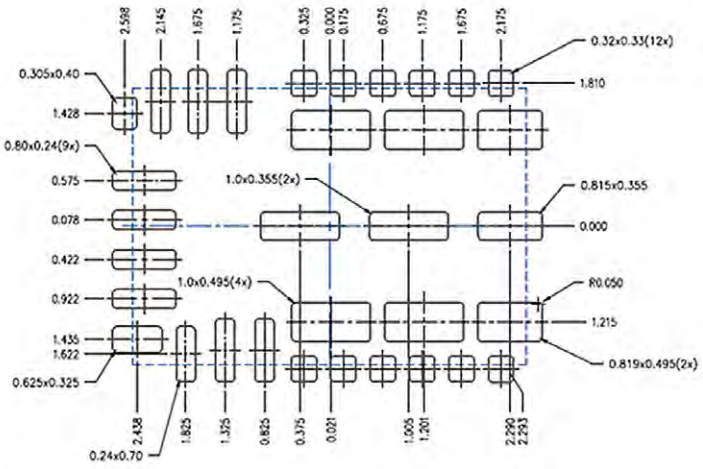


Figure 10: EPC23102 Stencil Design

4.1 Stand-off Height of a Small Pad (Pin 1 in Figure 9)

Equation 5 was used to calculate the stand-off height, which is estimated to be 46 µm. Figure 11 shows the respective areas that were used for the calculation, where the coefficient factor, k, is 0.45, and the stencil thickness, t, is 0.1 mm. Figure 12 shows the SEM cross-sectional results of Pin 1 post assembly, where the resulting stand-off height is measured to be 48 µm matching well the estimated stand-off height.

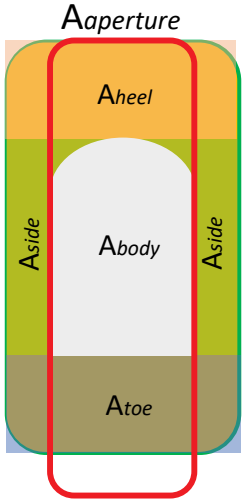


Figure 11: Illustration of solder area on a small pad where $A_{aperture}$ is to area of stencil opening over printing the land pattern as shown in the red box, $A_{aperture} = 0.19\ mm^2$. The area of the toe, $A_{toe} = 0.06\ mm^2$. The area of the body, $A_{body} = 0.09\ mm^2$. The total area of the sides, $A_{sides} = 0.03\ mm^2$. The area of the heel, $A_{heel} = 0.04\ mm^2$.

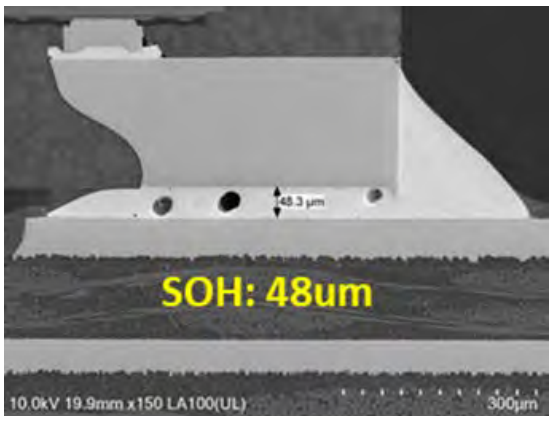


Figure 12: Actual Solder Stand-Off Height at Pin 2 of EPC23102 using 100 µm thick stencil.

4.2 Stand-off Height for a "L-shaped" Pad (Pin 13 in Figure 9)

Equation 5 was also used to estimate the stand-off height of a "L-shaped" exposed pad, where it was calculated to be 54 µm. Figure 13 shows the respective areas that were used for the calculation, where the coefficient factor, k, is 0.50, and the stencil thickness, t, is 0.1 mm. Figure 14 shows the SEM cross-sectional results of the pin 13 post reflow. The stand-off height is measured to be 52 µm, matching well with the estimated stand-off height.

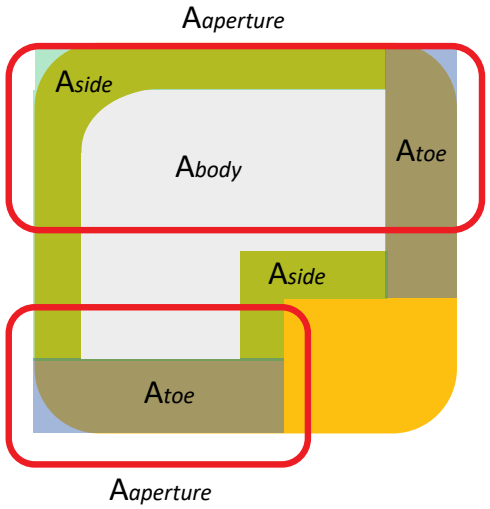


Figure 13: Illustration of solder area of a "L-shaped" pad where Aaperture is the total area of stencil opening over printing the land pattern as shown in the red boxes, Aaperture = 0.31 mm². The total area of the toe, A_{toe} = 0.12 mm². The area of the body, A_{body} = 0.16 mm². The total area of the sides, A_{sides} = 0.04 mm².

4.3 Stand-off Height for a Big Pad (Pin 10 in Figure 9)

Figure 15 shows the SEM cross-sectional results of the pin 10 post assembly, where the resulting stand-off height is measured to be 57 µm, precisely matching the estimated stand-off height. The stand-off height of a big pad is calculated to be 57 µm. Figure 16 shows the respective areas that were used for the calculation, where the coefficient factor, k, is 0.70, and the stencil thickness, t, is 0.1 mm.

Table 2 summarizes stand-off height prediction vs. the actual measurements. The package tilt is the stand-off height difference between the two opposite leads between Pin 13 to Pin 10. Table 2 shows that the tilt prediction is consistent with the actual cross-section measurements, further validating the design rule.

Stand-Off Height	PIN 2	PIN 13	PIN 10	TILT (P13 -P10)
Prediction	46 µm	54 µm	57 µm	3 µm
Actual	48 µm	52 µm	57 µm	5 µm

Table 2: EPC23102 Stand-Off Height Comparison

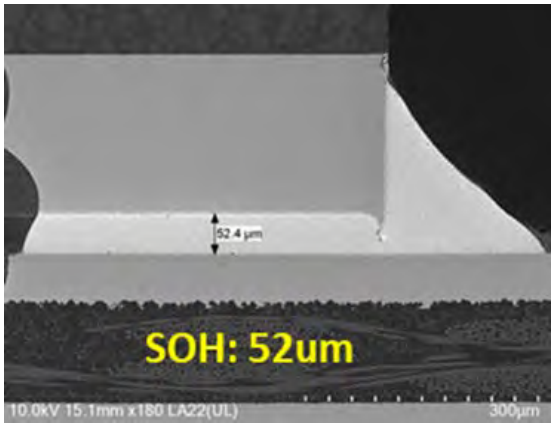


Figure 14: Actual Solder Stand-Off Height at Pin 13 of EPC23102 using 100 µm thick stencil.

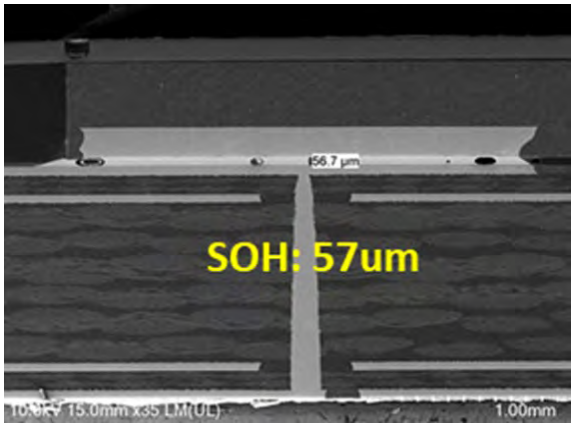


Figure 15: Actual Solder Stand-Off Height at Pin 10 of EPC23102 using 100 µm thick stencil.

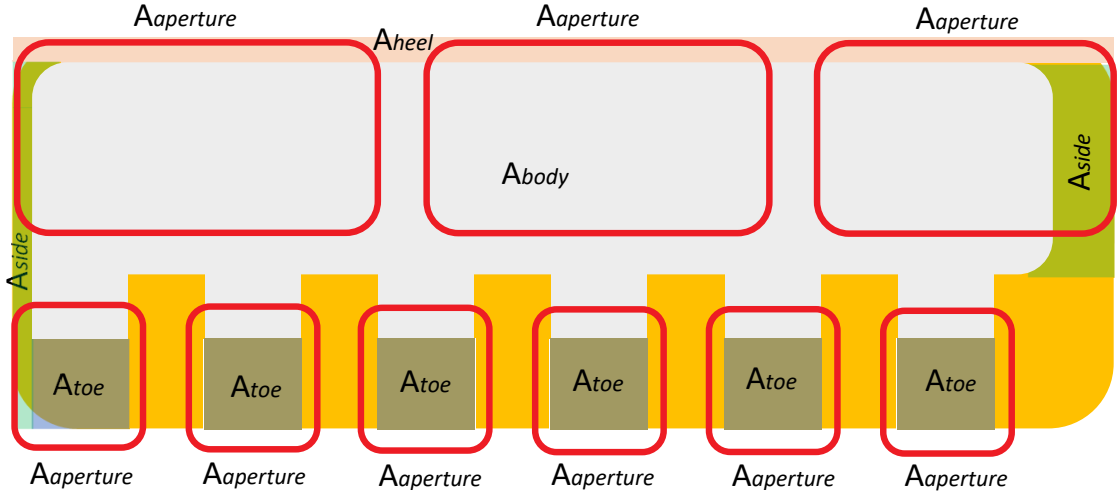


Figure 16: Illustration of solder area of a big-exposed pad where $A_{aperture}$ is the total area of stencil opening over printing the land pattern as shown in the red boxes, $A_{aperture}$ = 2.01 mm². The total area of the toe, A_{toe} = 0.38 mm². The area of the body, A_{body} = 1.85 mm². The total area of the sides, A_{sides} = 0.14 mm². The area of the heel, A_{heel} = 0.15 mm².

5. Case Study 2: A 3 x 5 mm Discrete PQFN Transistor EPC2302 [81] with 150 µm Thick Stencil

A 50% increase in stencil thickness increases the adhesion of solder paste on the aperture wall surface area, which reduces the percentage of transfer efficiency, yielding a lower coefficient factor. Figure 17 shows the bump layout of EPC2302, and Figure 18 is the 150 µm thick stencil recommendation based on the design rules.

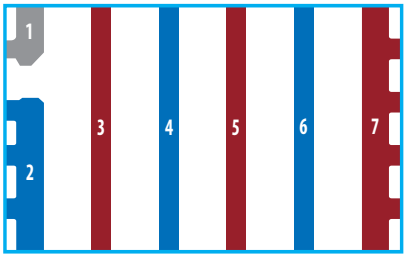


Figure 17: EPC2302 PQFN 3 x 5 mm bump layout

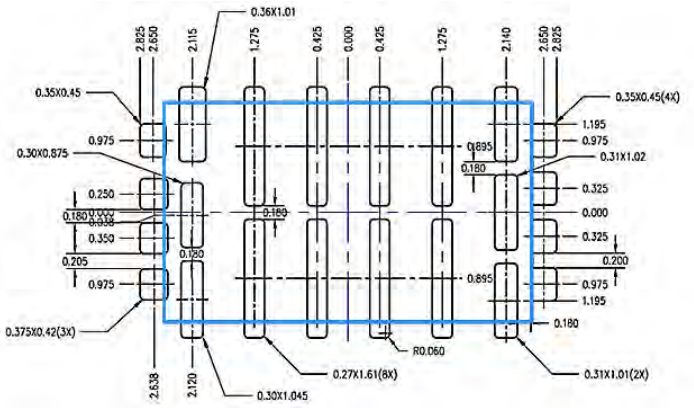


Figure 18: 150 µm stencil design for EPC2302

5.1 Stand-off Height of an "L-shaped" Pad in EPC2302 (Pin 1 in Figure 17)

The stand-off height of a "L-Shaped" pad is calculated to be 76 µm. Figure 19 shows the respective areas that were used for the calculation, where the coefficient factor, k, is 0.40, and the stencil thickness, t, is 0.15 mm. Figure 20 shows the SEM cross-sectional results of the pin 1 post assembly, where the resulting stand-off height is measured to be 81 µm matching reasonably well the estimated stand-off height.

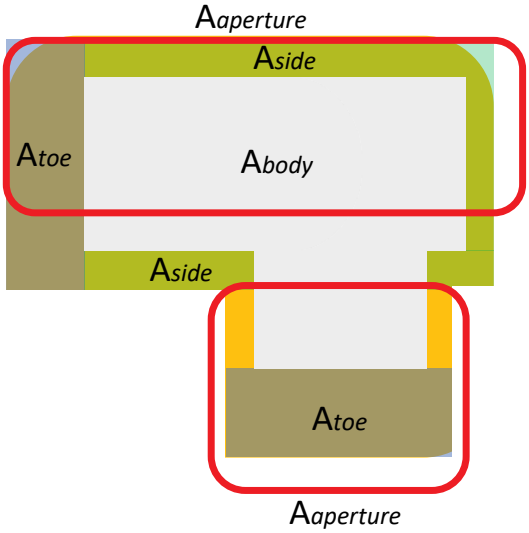


Figure 19: Illustration of solder area on an "L-shaped" pad where Aaperture is the total area of stencil opening over printing the land pattern as shown in the red boxes, $A_{aperture} = 0.52\ mm^2$. The total area of the toe, $A_{toe} = 0.13\ mm^2$. The area of the body, $A_{body} = 0.25\ mm^2$. The total area of the sides, $A_{sides} = 0.10\ mm^2$.

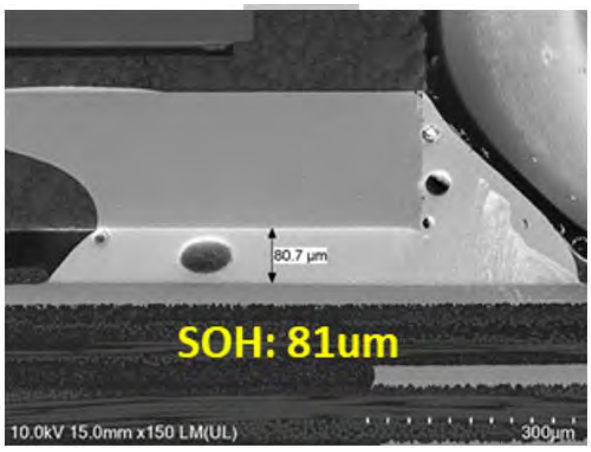


Figure 20: EPC2302 Actual Solder Stand-Off Height at Pin 1 using 150 µm thick stencil.

5.2 Stand-off Height for a Big Pad in EPC2302 (Pin 7 in Figure 17)

The stand-off height of a big-exposed pad is calculated to be 81 µm. Figure 21 shows the respective areas that were used for the calculation, where the coefficient factor, k, is 0.56, and the stencil thickness, t, is 0.15 mm. Figure 22 shows the SEM cross-sectional results of the pin 7 post assembly, where the resulting stand-off height is measured to be 76 µm, reasonably consistent with the estimated stand-off height.

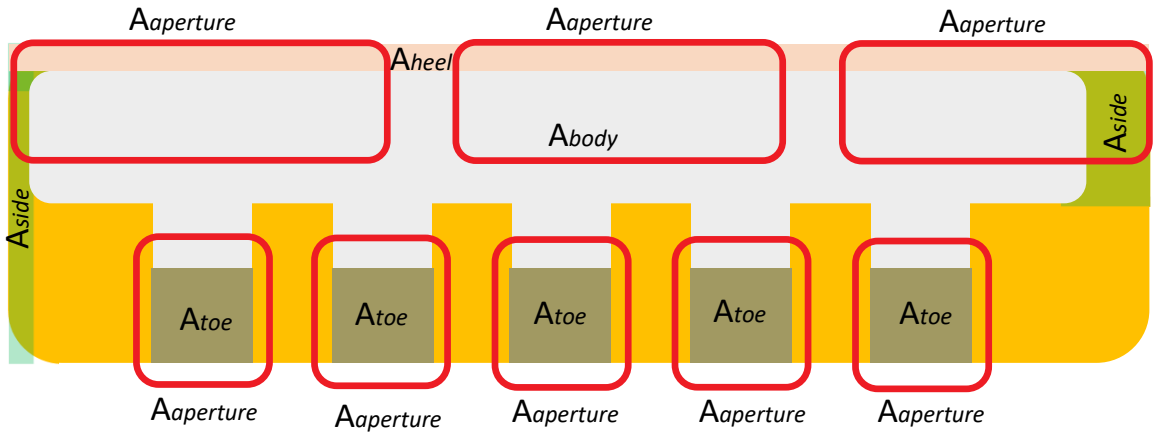


Figure 21: Illustration of solder area on a big pad where $A_{aperture}$ is the total area of stencil opening over printing the land pattern as shown in the red boxes, $A_{aperture} = 1.55\ mm^2$. The total area of the toe, $A_{toe} = 0.39\ mm^2$. The area of the body, $A_{body} = 1.1\ mm^2$. The total area of the sides, $A_{sides} = 0.08\ mm^2$. The area of the heel, $A_{heel} = 0.12\ mm^2$.

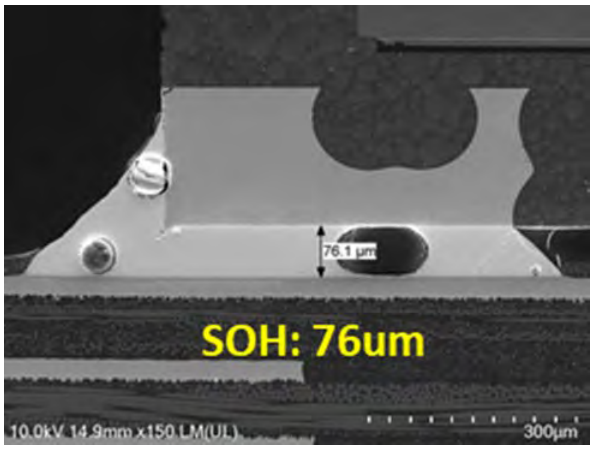


Figure 22: EPC2302 Actual Solder Stand-Off Height at Pin7 using 150 µm stencil thickness.

Table 3 summarize stand-off height prediction vs the actual measurements. Package tilt between the two opposite leads from Pin 1 to Pin 7 is small, showing the effectiveness of the design rule.

Stand-Off Height	PIN 1	PIN 7	TILT
Prediction	76 µm	81 µm	5 µm
Actual	81 µm	76 µm	5 µm

Table 3: EPC2302 Stand-Off Height Comparison using 150 µm stencil thickness.

6. Conclusion

By quantifying each solder component's volume, the stand-off height for pads of all sizes and shapes can be calculated. A stencil should be designed such that the stand-off heights calculated using Equation 5 are consistent across the part, which prevents die tilt and improves board level solder joint reliability.

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